CATIROC (Charge And Time Integrated Read Out Chip) is a complete read-out chip manufactured in AustriaMicroSystem (AMS) SiGe 0.35 µm technology, designed to read arrays of 16 photomultipliers (PMTs). The ASIC is composed of 16 independent channels that work in triggerless mode, auto-triggering on the single photo-electron (p.e.) (160 fC at PMT gain 10^6).
The main features are:

- 16 inputs for negative signals: each voltage input is sent into 2 low noise preamplifiers (high and low gain) with variable gain to use a common high voltage for the 16 PMTs
- Charge measurement: each preamplifier is followed by slow shapers with variable shaping time. Each one is sent to an analog memory with a depth of 2 to provide a charge measurement up to 100pC.
- Triggerless acquisition: a fast shaper (5ns) per channel is followed by a low offset discriminator to auto-trig down to 50 fC. The threshold is set by an internal 10-bit DAC (Digital to Analog Converter).
- Time measurement: a “time stamp” performed by a 26-bit counter at 40 MHz and a “fine time” obtained thanks to two TAC (Time to Amplitude Converter) ramps per channels.
- Two 10-bit Wilkinson ADCs (Analog to Digital Converter): to convert the charge and fine time values at 160MHz.
- A digital part manages all the acquisition, the conversion and the readout.

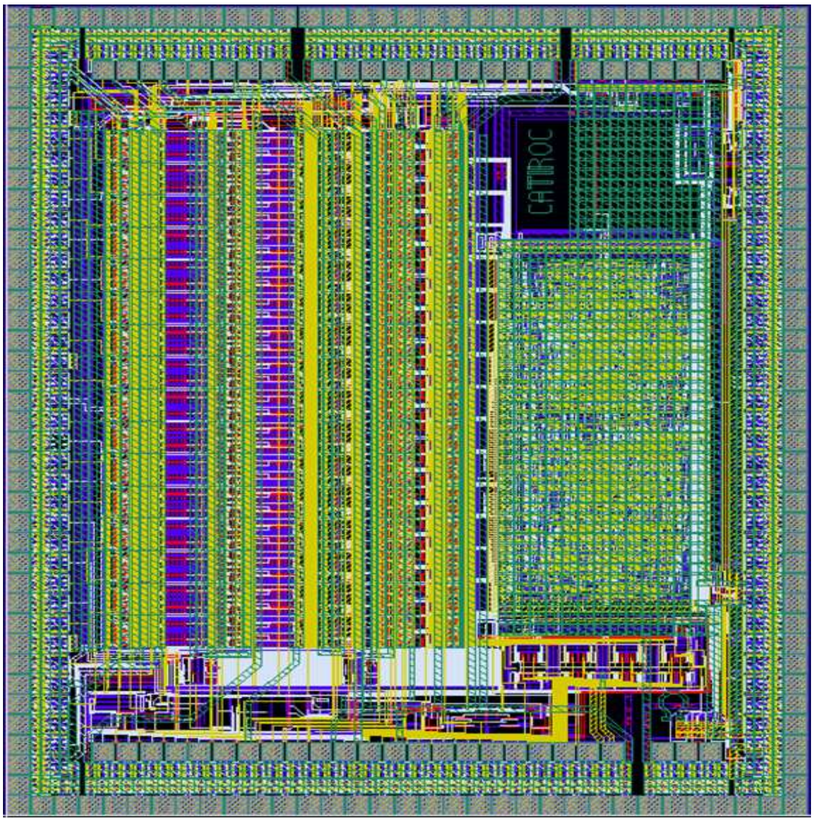

Figure 1 CATIROC Layout

Table 1 ASIC main parameters

Detector Read-Out	PMTs
Number of Channels	16
Signal Polarity	negative
Sensitivity	voltage
Timing	Time stamp: 26 bits counter @ 40 MHz Fine time: resolution 200 ps rms A TAC ramp for each channel
Charge Dynamic Range	160 fC up to 100pC
Trigger	Triggerless acquisition Noise= 9 fC; Minimum threshold ~ 65 fC
Digital	Conversion: 10 bits ADC at 160 MHz Two Read out at 80 MHz (Each one for 8 channels) Read out frame: 50 bits split in 2 frames of (29+21) bits 1st frame: coarse time= 26 bits ; Channel number= 3bits for the hit channels 2nd frame: Fine time=10 bits, Charge=10 bits, Gain=1 bit for same channels
Packaging & Dimension	TQFP 208 (28x28x1.4 mm) die : 3.3 mm x 4 mm
Power Consumption	21 mW/channel
Outputs	16 trigger outputs Or of the 16 triggers 16 slow shaper outputs 2 serial Data out (One for 8 channels)
Main Internal Programmable Features	Variable preamplifier gain per channel Variable shaping time and gain of the charge shaper Common trigger threshold adjustment Common charge threshold adjustment

Learn more about CATIROC

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1 General description

CATIROC has been designed in AMS SiGe 0.35 µm technology and integrates 16 identical channels dedicated to read out PMT pulses. It auto-triggers on the single photo-electron (p.e.) and sustains a dark noise rate of 20 kHz/channel. It provides a charge measurement over a dynamic range from 160 fC (1 p.e. at PMT gain of 10^6) up to 100 pC (~ 600 p.e.) (in case of default configuration, see paragraph 4.6). It also provides a timing measurement with an accuracy of 500 ps (200 ps rms) per channel. A gain adjustment per channel (over 8 bits) allows to compensate the non-uniformity of the 16 PMTs operated at the same high voltage. Only two lines of digital data running at 160 MHz come out.

The chip architecture is shown in figure 2. The ASIC is made of two main paths: a slow and a fast channel.

The slow channel is obtained by two input voltage preamplifiers with high and low gain respectively (PA HG and PA LG on figure 2). The gain of each channel can be set individually and can be adjusted on 8 bits thanks to a preamplifier feedback variable capacitor (values from 8 fF to 1 pF). This feature is implemented in order to compensate the gain non-uniformity of the 16 input PMTs operated at the same high voltage to reduce the cost of HV power supplies. Each preamplifier is followed by a slow shaper (SSH HG and SSH LG on figure 2) and two Track-and- Hold (T&H on figure 2) stages in order to provide a charge measurement. The slow shaper has a tunable shaping time up to 100 ns and variable gain obtained by a switchable resistors and capacitors. The two T&H work in a “ping-pong mode”: while the first value is digitized, a second slow shaper signal can be stored in a second capacitor. The HG T&H is followed by a “charge discriminator”. It compares the slow shaper HG maximum voltage value with a threshold (Charge threshold on figure 2) which is set by an internal 10-bit DAC common for the 16 channels. When the HG signal is saturated, the LG one is selected. One of these charge analog values is then converted by the internal 10-bit Wilkinson ADC operated at 160 MHz.

The fast channel is made by the high gain preamplifier followed by a fast shaper (5 ns) (FSH on figure 2) and a low offset discriminator to auto-trigger down to 50 fC (1/3 p.e.). Its threshold is set by an internal 10-bit DAC common for the 16 channels. The discriminator output signal (or trigger) is delayed to hold the shaper signal at its maximum value into the T&H. It is also used to manage two TACs (Time to Analog Converter) that convert the time in a voltage using two ramps of 25 ns. The time measurement is classically obtained by two paths: a “time stamp” performed by a 26-bit counter at 40 MHz and a “fine time” obtained thanks to two TAC ramps per channels converted by another 10-bit Wilkinson ADC.

All channels are handled independently by the digital part and only channels that have created triggers are digitized, transferred to the internal memory and then sent-out in a data-driven way.

The 16 discriminators, the “OR” of the 16 triggers and the analog shapers outputs are also available for peculiar applications.

A shift registers is used to send the configuration parameters (called slow control parameters) inside the chip. There are 328 Slow Control (SC) parameters which are loaded serially to control the chip (see table 3).

All the biases of each block are switchable by Slow Control and each bloc could be power off independently.

A "probe" register allows to observe the output of each analog selected bloc (preamplifier, fast or slow shaper) by an analog buffer output and some internal digital signals by two digital outputs (see table 4)

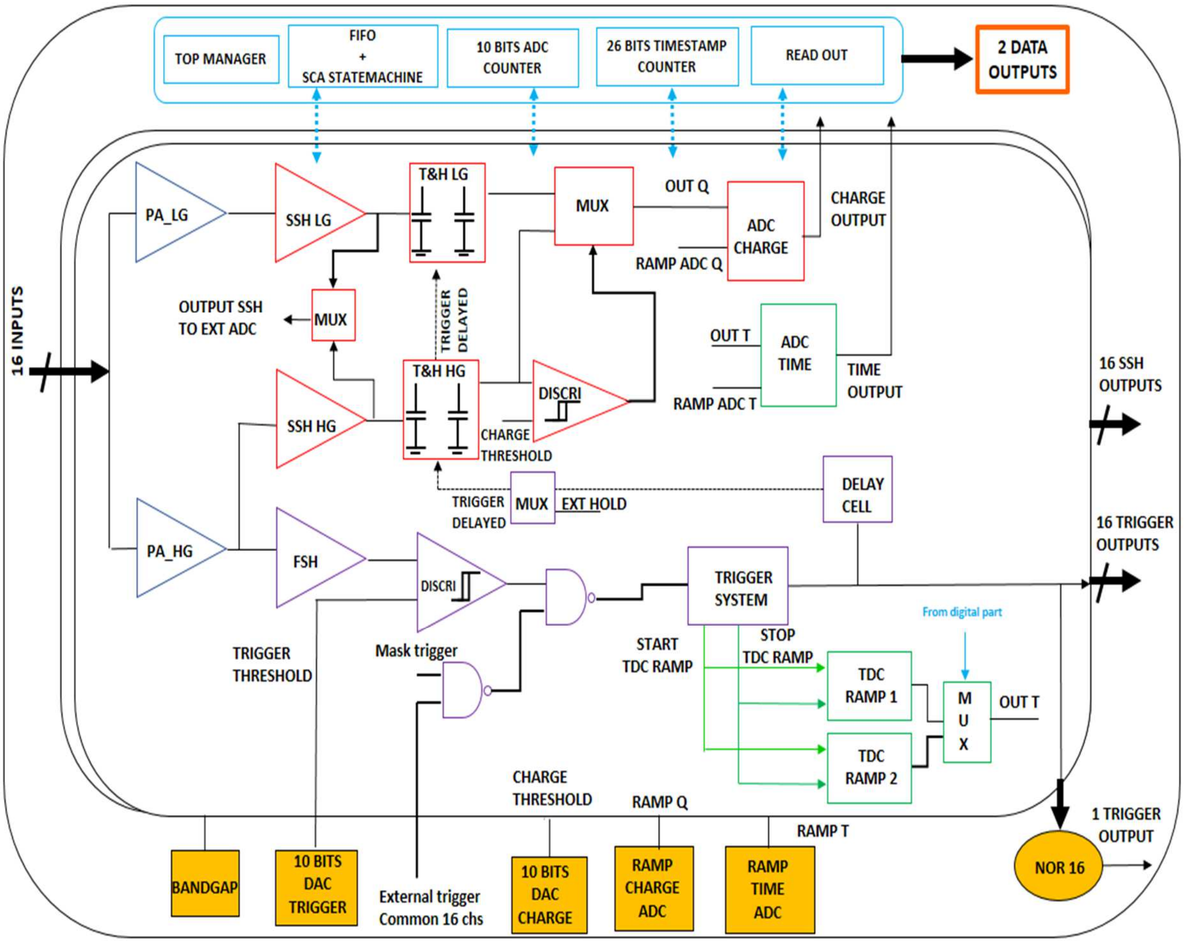

Figure 2 General ASIC block schematic

2 ASIC pinout

CATIROC is packaged in a TQFP 208.

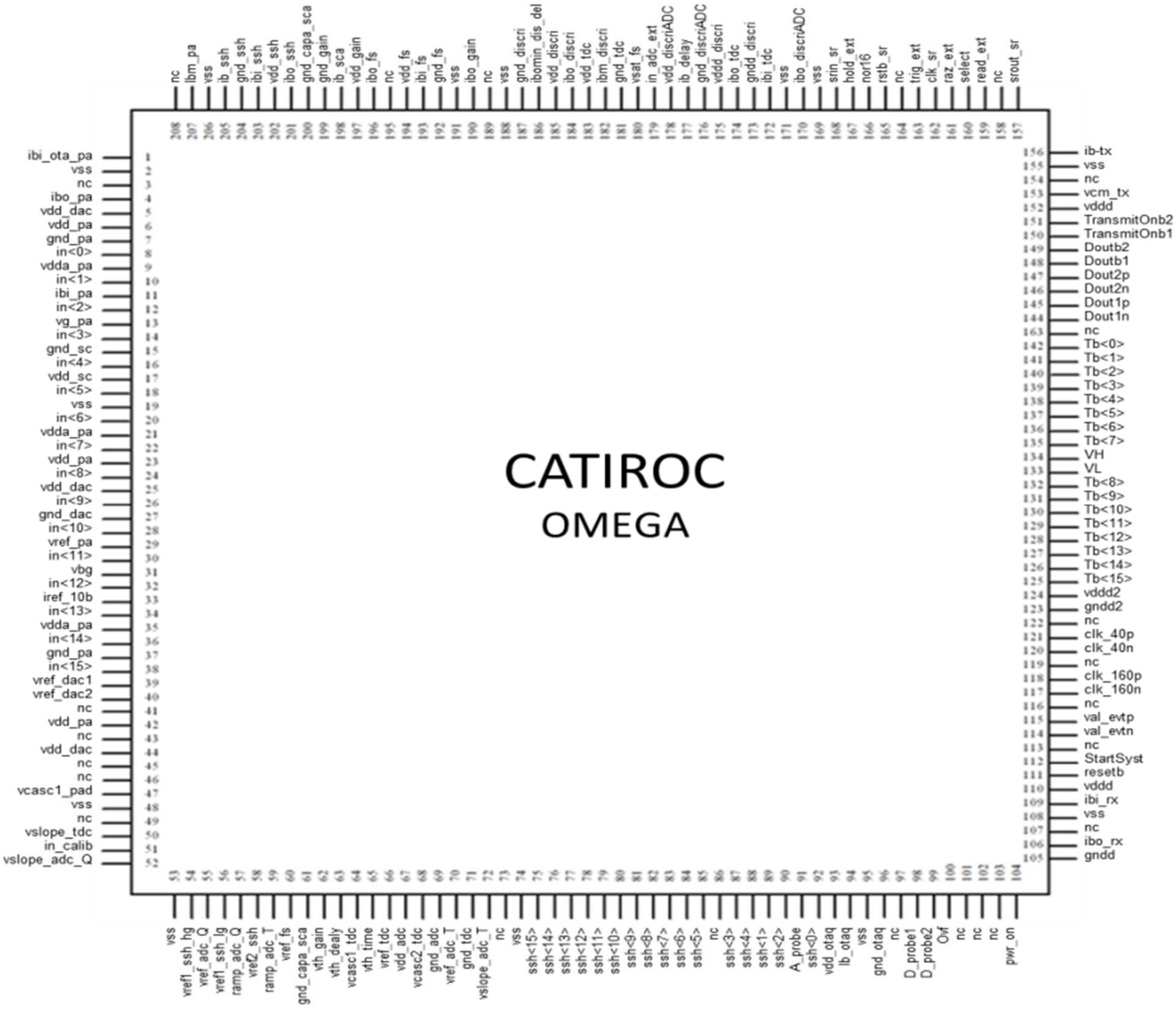

Figure 3 Pinout of CATIROC package

2.1 Pinout description

The ASIC pinout is described in table 2. The type of the pins is defined as follow: AB= Analog Bias, Pw=Power, AI= Analog Input, AO= Analog Output, DI = Digital Input, DO= Digital Output.

Table 2 Pinout description

1	ibi_ota_pa	AB	Preamp OTA input stage bias current	For measure or modifications	0.64V
2	vss	Pw	Substrate power supply	to ground	0 V
3	NC		no connected		
4	ibo_pa	AB	Preamp output stage bias current	For measure or modifications	1.2 V
5	vdd_dac	Pw	DAC power supply	to analog 3.3V (100nF)	3.3V
6	vdd_pa	Pw	Preamplifier power supply	to analog 3.3V (100nF)	3.3V
7	gnd_pa	Pw	Preamplifier Analog Ground	to ground	0V
8	in<0>	AI	Channel n°0 input	0 Ω in series +51 Ω to gnd	

9	vdda_pa	Pw	Preamp input stage power supply (very sensitive)	To vdda_pa (3.3V) (100nF)	3.3V
10	in<1>	AI	Channel n°1 input	0 Ω in series +51 Ω to gnd	
11	ibi_pa	AB	Preamplifier input stage bias current	For measure or modifications	1.4 V
12	in<2>	AI	Channel n°2 input	0 Ω in series +51 Ω to gnd	
13	vg_pa	AB	Preamplifier cascode voltage	For measure or modifications	1.8V
14	in<3>	AI	Channel n°3 input	0 Ω in series +51 Ω to gnd	
15	gnd_sc	Pw	Slow Control Analog Ground	to ground	0V
16	in<4>	AI	Channel n°4 input	0 Ω in series +51 Ω to gnd	
17	vdd_sc	Pw	Slow Control power supply	to analog 3.3V (100nF)	3.3V
18	in<5>	AI	Channel n°5 input	0 Ω in series +51 Ω to gnd	
19	vss	Pw	Substrate Power Supply	to ground	0V
20	in<6>	AI	Channel n°6 input	0 Ω in series +51 Ω to gnd	
21	vdda_pa	Pw	Preamp input stage power supply (very sensitive)	To vdda_pa (3.3V) (100nF)	3.3V
22	in<7>	AI	Channel n°7 input	0 Ω in series +51 Ω to gnd	
23	vdd_pa	Pw	Preamplifier power supply	to analog 3.3V (100nF)	3.3V
24	in<8>	AI	Channel n°8 input	0 Ω in series +51 Ω to gnd	
25	vdd_dac	Pw	DAC power supply	to analog 3.3V (100nF)	3.3V
26	in<9>	AI	Channel n°9 input	0 Ω in series +51 Ω to gnd	
27	gnd_dac	Pw	DAC Analog Ground	to ground	0V
28	in<10>	AI	Channel n°10 input	0 Ω in series +51 Ω to gnd	
29	vref_pa	AB	Preamplifier voltage reference	For measure or modifications	1V
30	in<11>	AI	Channel n°11 input	0 Ω in series +51 Ω to gnd	
31	vbg	AB	Bandgap voltage output	For measurement	2.5V
32	in<12>	AI	Channel n°12 input	0 Ω in series +51 Ω to gnd	
33	iref_10bdac	AB	DAC current reference	For measure or modifications	2.26V
34	in<13>	AI	Channel n°13 input	0 Ω in series +51 Ω to gnd	
35	vdda_pa	Pw	Preamp input stage power supply (very sensitive)	To vdda_pa (3.3V) (100nF)	3.3V
36	in<14>	AI	Channel n°14 input	0 Ω in series +51 Ω to gnd	
37	gnd_pa	Pw	Preamplifier Analog Ground	to ground	0V
38	in<15>	AI	Channel n°15 input	0 Ω in series +51 Ω to gnd	
39	vref_dac_trigger	AB	10-bit DAC trigger voltage reference	For measure or modifications	1V
40	vref_dac_gain	AB	10-bit DAC gain voltage reference	For measure or modifications	1V
41	NC		no connected		
42	vdd_pa	Pw	Preamplifier power supply	to analog 3.3V (100nF)	3.3V
43	NC		no connected		
44	vdd_dac	Pw	DAC power supply	to analog 3.3V (100nF)	3.3V
45,46	NC		no connected		
47	vcasc1_tac_pad	AB	TAC cascode voltage before OTA	For measure or modifications	1.2V
48	vss	Pw	Substrate power supply	to ground	0V
49	NC		no connected		
50	vslope_tac	AB	voltage of the TAC ramp slope	For measure or modifications	0.35V
51	in_calib	AI	Calibration input	External connector for signal	
52	vslope_adc_Q	AB	Volt. of the charge ADC ramp slope	To add 150k Ω to gnd	0.46 V
53	vss	Pw	Substrate supply	to ground	0V
54	vref1_ssh_hg	AB	Slow shaper HG 1st stage ref. volt.	For measure or modifications	1V
55	vref_adc_Q	AB	voltage ref. of ramp for charge ADC	For measure or modifications	0.96V
56	vref1_ssh_lg	AB	Slow shaper LG 1st stage ref. volt.	For measure or modifications	1V
57	ramp_adc_Q	AO	Charge ADC ramp	For visualization	
58	vref2_ssh	AB	voltage ref. of slow shapers HG and LG 2nd stage	For measure or modifications	1V
59	ramp_adc_T	AO	Time ADC ramp	For visualization	
60	vref_fs	AB	voltage reference of fast shaper	For measure or modifications	1.87V
61	gnd_capa_sca	Pw	ground for capacitances of the analog memory	to ground	0 V

62	vth_gain	AB	Threshold voltage for gain discri (10bit DAC2)	For visualization	
63	vth_delay	AB	Threshold voltage for delay discriminator	For visualization	1.75V
64	vcasc1_tac	AB	TAC cascode voltage after OTA	For visualization	1.2V
65	vth_trigger	AB	Threshold voltage for trigger discri. (10bit DAC1)	For visualization	
66	vref_tac	AB	voltage reference of TAC	For measure or modifications	1V
67	vdd_adc	Pw	Ramp ADC power supply	to analog 3.3V (100nF)	3.3V
68	vcasc2_tac	AB	2nd TAC cascode voltage	For measure or modifications	1.7V
69	gnd_adc	Pw	Ramp ADC Analog Ground	to ground	0V
70	vref_adc_T	Pw	voltage ref. of ramp for time ADC	To add 410kΩ to VBG pin31	1.14 V
71	gnd_tac	Pw	Ramp TAC Analog Ground	to ground	0V
72	vslope_adc_T	AB	voltage of the time ADC ramp slope	For measure or modifications	
73	NC		no connected		
74	vss	Pw	Substrate power supply	to ground	0 V
75 to 85	ssh<15:5>	AO	Slow Shaper outputs for channel n° 15 to 5	To external buffers or ADC	
86	NC		no connected		
87	ssh<3>	AO	Slow Shaper output for channel n°3	To external buffers or ADC	
88	ssh<4>	AO	Slow Shaper output for channel n°4	To external buffers or ADC	
89	ssh<1>	AO	Slow Shaper output for channel n°1	To external buffers or ADC	
90	ssh<2>	AO	Slow Shaper output for channel n°2	To external buffers or ADC	
91	A_probe	AO	Analog probe output	To external buffer for debug	
92	ssh<0>	AO	Slow Shaper output for channel n° 0	To external buffers or ADC	
93	vdd_otaq	Pw	Analog output buffers power supply	to analog 3.3V (100nF)	3.3V
94	ib_otaq	AB	Analog output buffers bias current	For measure or modifications	1V
95	vss	Pw	Substrate power supply	to ground	0V
96	gnd_otaq	Pw	Output buffers Analog Ground	to ground	0V
97	NC		no connected		
98	D_probe1	DO	DIGITAL PROBE n°1 output	To FPGA (custom bank) for debug	Custom CMOS
99	D_probe2	DO	DIGITAL PROBE n°2 output	To FPGA (custom bank) for debug	Custom CMOS
100	Ovf	DO	Overflow of Timestamp counter (active high)	To FPGA (custom bank)	Custom CMOS
101 to 103	NC		no connected		
104	pwr_on	DI	Power Pulsing Control (active high)	From FPGA	CMOS
105	gndd	Pw	Full custom digital part ground	to ground	0V
106	ibo_rx	AB	LVDS receiver output stage bias	For measure or modifications	1.3V
107	NC		no connected		
108	vss	Pw	Substrate power supply	to ground	0 V
109	ibi_rx	AB	LVDS receivers input stage bias	For measure or modifications	2V
110	vddd	Pw	Full custom digital part power supply	to digital 3.3V (100nF)	3.3V
111	resetb	DI	Reset for digital part (active low)	From FPGA	CMOS
112	StartSyst	DI	Start Acquisition and Timestamp counter (active high)	From FPGA	CMOS
113	NC		no connected		
114 **115**	val_evtn val_evtp	DI - DI+	External gate for triggers : LVDS differential inputs (active high)	From FPGA	LVDS
116	NC		no connected		
117 **118**	clk_160n clk_160p	DI - DI+	160MHz clock for ADC : LVDS differential inputs	From FPGA	LVDS
119	NC		no connected		
120 **121**	clk_40n clk_40p	DI - DI+	40MHz clock for timestamp : LVDS differential inputs	From FPGA	LVDS
122	NC		no connected		
123	gndd2	Pw	Digital Ground	to ground	0V
124	vddd2	Pw	Digital Power Supply	to digital 3.3V (100nF)	3.3V

125 to 132	Tb<15: 8>	DO	Channel n° 15 to 8 trigger outputs : active low	To FPGA (custom bank)	Custom CMOS
133	VL	Pw	Output buffers lowest power supply	to ground	0V
134	VH	Pw	Output buffers highest power supply : chosen to define custom CMOS (same as FPGA bank)	To 1.8, 2.5 or 3.3V (same as the FPGA bank used) = custom CMOS	1.8, 2.5 or 3.3V
135 to 142	Tb<7 : 0>	DO	Channel n° 7 to 0 trigger outputs : active low	To FPGA (custom bank)	Custom CMOS
143	NC		no connected		
144 **145**	Dout1n Dout1p	DO - DO +	1st Data Serial Output for channels n° 0 to7 : LVDS differential outputs	To FPGA (LVDS bank)	LVDS
146 **147**	Dout2n Dout2p	DO - DO +	2nd Data Serial Output for channels n° 8 to 15 :LVDS differential outputs	To FPGA (LVDS bank)	LVDS
148	Doutb1	DO	1st Data Serial Output in open collector mode	To FPGA (custom bank) 100 Ω to VH	Custom CMOS
149	Doutb2	DO	2nd Data Serial Output in open collector mode	To FPGA (custom bank) 100 Ω to VH	Custom CMOS
150	TransmitOnb1	DO	Readout of Dout1 active when 0 (open collector)	To FPGA (custom bank) 100 Ω to VH	Custom CMOS
151	TransmitOnb2	DO	Readout of Dout2 active when 0 (open collector)	To FPGA (custom bank) 100 Ω to VH	Custom CMOS
152	vddd	Pw	Full custom digital power supply	to digital 3.3V (100nF)	3.3V
153	vcm_tx	AB	Common mode voltage for LVDS transmitters	For measure or modifications	1.2V
154	NC		no connected		
155	vss	Pw	Substrate power supply	to ground	0 V
156	ib_tx	AB	LVDS transmitters bias current	For measure or modifications	0.8V
157	srout_sr	DO	PROBE or SLOW CONTROL shift register output	To FPGA	CMOS
158	NC		no connected		
159	read_ext	DI	External "read" command input	From FPGA only for debugging. No internal pull down : 100k to gnd.	CMOS
160	select	DI	PROBE (0) or SLOW CONTROL(1) register selection	From FPGA	CMOS
161	raz_ext	DI	External reset command input : active high	From FPGA only for debugging. No internal pull down : 100k to gnd.	CMOS
162	clk_sr	DI	Clock for PROBE or SLOW CONTROL register	From FPGA	CMOS
163	trig_ext	DI	External "trigger" command input	From FPGA	CMOS
164	NC		no connected		
165	rstb_sr	DI	Reset for PROBE or SC registers (active low)	From FPGA	CMOS
166	NOR16	DO	"NOR" of the 16 triggers output (active low)	To FPGA (custom bank) 100 Ω to VH	Custom CMOS
167	hold_ext	DI	External "hold" command input	From FPGA only for debugging	CMOS
168	srin_sr	DI	PROBE or SC shift register input	From FPGA	CMOS
169	vss	Pw	Substrate power supply	to ground	0 V
170	ibo_discriADC	AB	ADC discriminator output stage bias current	For measure or modifications	2.3V
171	vss	Pw	Substrate power supply	to ground	0 V
172	ibi_tac	AB	TAC input stage bias current	For measure or modifications	2.4V
173	gndd_discri	Pw	Digital part of discriminator ground	to ground	0V
174	ibo_tac	AB	TAC output stage bias current	For measure or modifications	0.8V
175	vddd_discri	Pw	Digital part of discri. power supply	to analog 3.3V (100nF)	3.3V
176	gnd_discriADC	Pw	Discriminator ADC Ground	to ground	0V
177	ib_delay	AB	Delay cell bias current	For measure or modifications	0.6V
178	vdd_discriADC	Pw	ADC Discriminator power supply	to analog 3.3V (100nF)	3.3V

179	in_adc_ext	AI	External input to test internal ADC	External connector only for debugging	
180	vsat_fs	AB	Fast Shaper saturation voltage	For measure or modifications	1.8V
181	gnd_tac	Pw	TAC ramp Analog Ground	to ground	0V
182	Ibm_discri	AB	Discriminator middle stage bias current	For measure or modifications	0.6V
183	vdd_tac	Pw	TAC Ramp power supply	to analog 3.3V (100nF)	3.3V
184	ibo_discri	AB	Discriminator output stage bias current	For measure or modifications	1.4V
185	vdd_discri	Pw	Discriminator power supply	to analog 3.3V (100nF)	3.3V
186	ibomin_delay	AB	Delay discriminator bias current	For measure or modifications	2.7V
187	gnd_discri	Pw	Discriminator Ground	to ground	0V
188	vss	Pw	Substrate power supply	to ground	0 V
189	NC		no connected		
190	ibo_gain	AB	Gain discriminator bias current	For measure or modifications	2.5V
191	vss	Pw	Substrate power supply	to ground	0 V
192	gnd_fs	Pw	Fast shaper Ground	to ground	0V
193	ibi_fs	AB	Fast Shaper input stage bias current	Necessary to dd an external resistor 30 kΩ to gnd	0.8V 0.7 V
194	vdd_fs	Pw	Fast Shaper power supply	to analog 3.3V (100nF)	3.3V
195	NC		no connected		
196	ibo_fs	AB	Fast Shaper output stage bias current	For measure or modifications	0.8V
197	vdd_gain	Pw	Gain discriminator power supply	to analog 3.3V (100nF)	3.3V
198	ib_sca	AB	Buffer of the analog memory bias	For measure or modifications To add an external resistor 58k Ohm to gnd	0.9V
199	gnd_gain	Pw	Gain discriminator Ground	to ground	0V
200	gnd_capa_sca	Pw	ground for capacitences of the analog memory	to ground	0 V
201	ibo_ssh	AB	Slow Shaper output stage bias	For measure or modifications	0.7V
202	vdd_ssh	Pw	Slow Shaper Power Supply	to analog 3.3V (100nF)	3.3V
203	ibi_ssh	AB	Slow Shaper input stage bias	For measure or modifications	0.7V
204	gnd_ssh	Pw	Slow Shaper Analog Ground	to ground	0V
205	ib_ssh	AB	OTA of slow shaper bias current	For measure or modifications	0.7V
206	vss	Pw	Substrate power supply	to ground	0 V
207	ibm_pa	AB	Preamplifier middle stage bias current	For measure or modifications	2V
208	NC		no connected		

2.2 ASIC programmable parameters

2.2.1 Slow Control Register

The slow control (SC) register is used to load the ASIC configuration parameters. It is a shift register composed of n flip flops (n = 328 in CATIROC: Bit 1 = enable_input_test_ch0 and Bit 328 = switch_2mA_inTX_bias). Data (pin168 : srin_sr) are stored in flip flops on leading edge of the clock (pin 162 : clk_sr) and shifted at each clock cycle as seen on figure 4. (Bit 1 is the last bit sent and Bit 328 the first one). Sending twice, the data could be verified by reading pin 157 (srout_sr). A reset command (pin 165 : rstb_sr,) active on low level, loads the default value on each parameter (see table 3).

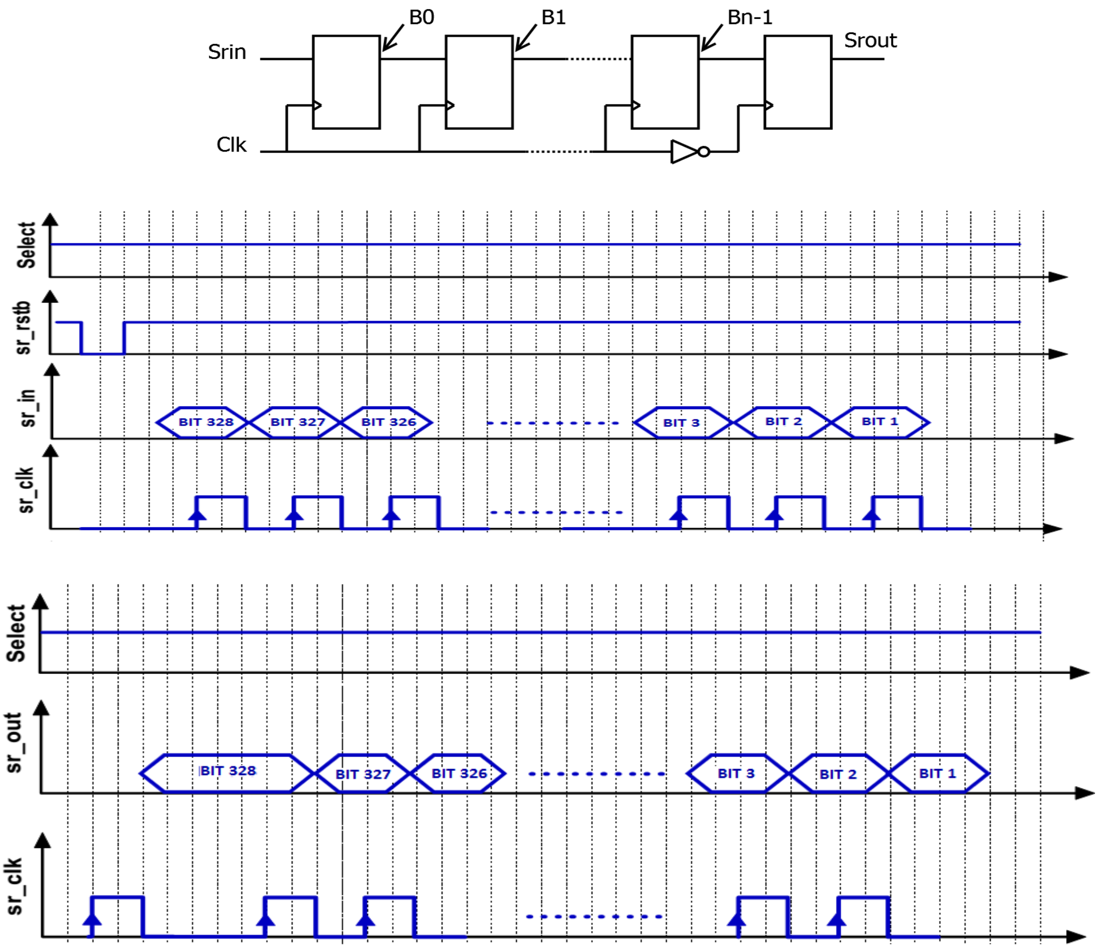

Figure 4 Slow control schematic and chronogram

The 328 slow control register parameters are described in table3 below.

Table 3 Slow control register parameters

1	Enable input test _ch 0	test_input in channel n°0	0 (OFF)
2	Enable input test _ch 1	test_input in channel n°1	0 (OFF)
3	Enable input test _ch 2	test_input in channel n°2	0 (OFF)
4 to 15	…	… idem for channels 3 to 14	…
16	Enable input test _ch 15	test_input in channel n°15	0 (OFF)
17	sw_cf<7>_ch0	Choice of preamp feedback capacitance to set the gain of channel 0: 1 pF (G=5) (common to HG and LG)	0 (OFF)
18	sw_cf<6>_ch0	0.5 pF (G=10) (common to HG and LG)	0 (OFF)
19	sw_cf<5>_ch0	0.25 pF (G=20) (common to HG and LG)	1 (ON)
20	sw_cf<4>_ch0	0.125 pF (G=40) (common to HG and LG)	0 (OFF)
21	sw_cf<3>_ch0	0.062 pF (G=80) (common to HG and LG)	0 (OFF)
22	sw_cf<2>_ch0	0.031 pF (G=160) (common to HG and LG)	0 (OFF)
23	sw_cf<1>_ch0	0.015 pF (G=320) (common to HG and LG)	0 (OFF)
24	sw_cf<0>_ch0	0.008 pF (G=640) (common to HG and LG)	0 (OFF)
25	Sw_off_PA_HG_ch0	Disable high gain preamp of channel 0	1 (ON)
26	Sw_off_PA_LG_ch0	Disable low gain preamp of channel 0	1 (ON)

27	sw_cf<7>_ch1	Choice of preamp feedback capacitance to set the gain of channel 1 : 1 pF (G=5) (common to HG and LG)	0 (OFF)
28	sw_cf<6>_ch1	0.5 pF (G=10) (common to HG and LG)	0 (OFF)
29	sw_cf<5>_ch1	0.25 pF (G=20) (common to HG and LG)	1 (ON)
30	sw_cf<4>_ch1	0.125 pF (G=40) (common to HG and LG)	0 (OFF)
31	sw_cf<3>_ch1	0.062 pF (G=80) (common to HG and LG)	0 (OFF)
32	sw_cf<2>_ch1	0.031 pF (G=160) (common to HG and LG)	0 (OFF)
33	sw_cf<1>_ch1	0.015 pF (G=320) (common to HG and LG)	0 (OFF)
34	sw_cf<0>_ch1	0.008 pF (G=640) (common to HG and LG)	0 (OFF)
35	Sw_off_PA_HG_ch1	Disable high gain preamp of channel 1	1 (ON)
36	Sw_off_PA_LG_ch1	Disable low gain preamp of channel 1	1 (ON)
37 to 166	…	… idem for channels 2 to 14	…
167	sw_cf<7>_ch15	Choice of preamp feedback capacitance to set the gain of channel 15 : 1 pF (G=5) (common to HG and LG)	0 (OFF)
168	sw_cf<6>_ch15	0.5 pF (G=10) (common to HG and LG)	0 (OFF)
169	sw_cf<5>_ch15	0.25 pF (G=20) (common to HG and LG)	1 (ON)
170	sw_cf<4>_ch15	0.125 pF (G=40) (common to HG and LG)	0 (OFF)
171	sw_cf<3>_ch15	0.062 pF (G=80) (common to HG and LG)	0 (OFF)
172	sw_cf<2>_ch15	0.031 pF (G=160) (common to HG and LG)	0 (OFF)
173	sw_cf<1>_ch15	0.015 pF (G=320) (common to HG and LG)	0 (OFF)
174	sw_cf<0>_ch15	0.008 pF (G=640) (common to HG and LG)	0 (OFF)
175	Sw_off_PA_HG_ch15	Disable high gain preamp of channel 15	1 (ON)
176	Sw_off_PA_LG_ch15	Disable low gain preamp of channel 15	1 (ON)
177	Pw_ON_PA_HG_EN	Enable high gain preamp of all channels	10(ON)
178	Pw_ON_PA_HG_PP	Force ON orPower pulsing mode (table 5 in § 2.2.3)	
179	Pw_ON_PA_LG_EN	Enable low gain preamp of all channels	10 (ON)
180	Pw_ON_PA_LG_PP	Force ON or Power pulsing mode (table 5 in § 2.2.3)	
181	Pw_ON_SSH_HG_EN	Enable high gain slow shaper of all channels	10 (ON)
182	Pw_ON_SSH_HG_PP	Force ON or Power pulsing mode (table 5 in § 2.2.3)	
183	cmd_g_hg<1>	Gain choice of 1^{st} stage of slow shaper high gain	00
184	cmd_g_hg<0>	(See table 6 in paragraph 3.3)	(Rf1 = 64K)
185	cmd_rc_hg<2>	Time constant choice of 2^{nd} stage of slow shaper high gain (See table 6 in paragraph 3.3) : cmd_rc<2>=1 →100ns ; cmd_rc<1>=1 →50ns ; cmd_rc<0>=1 →25ns	010 (RC= 50ns)
186	cmd_rc_hg<1>		
187	cmd_rc_hg<0>		
188	Pw_ON_SSH_LG_EN	Enable low gain slow shaper of all channels	10 (ON)
189	Pw_ON_SSH_LG_PP	Force ON or Power pulsing mode (table 5 in § 2.2.3)	
190	cmd_g_lg<1>	Gain choice of 1^{st} stage of slow shaper low gain	00
191	cmd_g_lg<0>	(See table 6 in paragraph 3.3)	(Rf1 = 64K)
192	cmd_rc_lg<2>	Time constant choice of 2^{nd} stage of slow shaper low gain (See table 6 in paragraph 3.3) : cmd_rc<2>=1 →100ns ; cmd_rc<1>=1→50ns ; cmd_rc<0>=1 →25ns	010 (RC= 50ns)
193	cmd_rc_lg<1>		
194	cmd_rc_lg<0>		
195	cmd_rcg_hg<2>	Feedback capacitance choice of 1^{st} stage of slow shaper high gain : cmd_rcg<2>=1 →6.24pF ; cmd_rc<1>=1→3.12pF ; cmd_rc<0>=1 →1.56pF (See table 6 in paragraph 3.3)	001 (Cf1= 1.5pF)
196	cmd_rcg_hg<1>		
197	cmd_rcg_hg<0>		
198	cmd_rcg_lg<2>	Feedback capacitance choice of 1^{st} stage of slow shaper low gain : cmd_rcg<2>=1 →6.24pF ; cmd_rc<1>=1→3.12pF ; cmd_rc<0>=1 →1.56pF (See table 6 in paragraph 3.3)	001 (Cf1= 1.5pF)
199	cmd_rcg_lg<1>		
200	cmd_rcg_lg<0>		
201	Pw_SCA_EN	Enable SCA buffers for all channels	1 0(ON)
202	Pw_SCA_PP	Force ON or Power pulsing mode (table 5 in § 2.2.3)	
203	Gain_mode_selection	Select gain mode : Forced (0) or auto (1)	1 (Auto)
204	Pw_gain_discri_EN	Enable discriminator of gain for all channels	10 (ON)
205	Pw_gain_discri_PP	Force ON or Power pulsing mode (table 5 in § 2.2.3)	
206	Pw_fast_shaper_EN	Enable fast shaper for all channels	10 (ON)
207	Pw_fast_shaper_PP	Force ON or Power pulsing mode (table 5 in § 2.2.3)	

208	HOLDb mode selection	Select internal (0) or external (1) holdb signal for all channels	0 (internal)
209	Pw_trigger_discri_EN	Enable discriminator of trigger for all channels	10 (ON)
210	Pw_trigger_discri_PP	Force ON or Power pulsing mode (see table 5 in § 2.2.3)	
211	Pw_TAC_EN	Enable TAC bloc for all channels	10 (ON)
212	Pw_TAC_PP	Force ON or Power pulsing mode (table 5 in § 2.2.3)	
213	Pw_Q_ADC_EN	Enable Charge ADC for all channels	10 (ON)
214	Pw_Q_ADC_PP	Force ON or Power pulsing mode (table 5 in § 2.2.3)	
215	Pw_T_ADC_EN	Enable Time ADC for all channels	10 (ON)
216	Pw_T_ADC_PP	Force ON or Power pulsing mode (table 5 in § 2.2.3)	
217	Sel_data <0>	Select input data for charge and time ADCs :	00 : Q and T
218	Sel_data <1>	00 : Q and T ; 01 : HG and LG charge;10 : T and Q ; 11 : ADCs calibration	
219	Pw_DAC_delay_EN	Enable DAC delay for all channels	10 (ON)
220	Pw_DAC_delay_PP	Force ON or Power pulsing mode DAC delay all chs	
221 to 228	Delay<7: 0>	Delay value (from MSB to LSB). Common for all channels	00010010 : del<4>+del<1>
229	Mask_trigger_discri_ch0	mask of the channel 0 discri_trigger : 0= no mask, 1= masked	0 (no mask)
230	Mask_trigger_discri_ch1	mask of the channel 1 discri_trigger : 0= no mask, 1= masked	0 (no mask)
231 to 243	…	……. idem for channels 2 to 14	0 (no mask)
244	Mask_ trigger _discri_ch15	mask of the channel 15 discri_trigger : 0= no mask, 1= masked	0 (no mask)
245	SSH to PAD ch0	choice high (0) or low (1) gain slow shaper sent to pad for channel 0	0 (HG)
246	Force_gain_ch0	force low (0) or high (1) gain for ch. 0 if BIT 203= 0	0 (LG)
247	SSH to PAD ch1	choice high (0) or low (1) gain slow shaper sent to pad for channel 1	0 (HG)
248	Force_gain_ch1	force low (0) or high (1) gain for ch. 1 if BIT 203= 0	0 (LG)
249 to274	…	… idem for channels 2 to 14	…
275	SSH to PAD ch15	choice high (0) or low (1) gain slow shaper sent to pad for channel 15	0(HG)
276	Force_gain_ch15	force low (0) or high (1) gain for ch. 15 if BIT 203= 0	0(LG)
277	Pw_DAC_EN	Enable DACs	10 (ON)
278	Pw_DAC_PP	Force ON or Power pulsing mode (table 5 in § 2.2.3)	
279 to288	discri_trigger : B<9:0>	10-bit DAC (MSB to LSB) for discri_trigger threshold	No default value
289 to298	discri_gain : B<9:0>	10-bit DAC (MSB-LSB) for discri_gain threshold	No default value
299	Pw_Ramp_ADC_Q_EN	Enable Ramp ADC charge	10 (ON)
300	Pw_Ramp_ADC_Q_PP	Force ON or Power pulsing mode (table 5 in § 2.2.3)	
301	Sw_compensation_Ramp _ADC_Q	add compensated switches on charge ADC ramp (0= switch, 1=no sw)	1 (no switch)
302	Ramp_ADC_Q_slope	choice charge ADC ramp slope for 160MHz(0) or 80MHZ(1)	0 (160 MHz)
303	Pw_Ramp_ADC_T_EN	Enable Ramp of time ADC	10 (ON)
304	Pw_Ramp_ADC_T_PP	Force ON or Power pulsing mode (table 5 in § 2.2.3)	
305	Sw_compensation_Ramp _ADC_T	add compensated switch on Time ADC ramp (0= switch, 1=no sw)	1 (no switch)
306	Ramp_ADC_T_slope	choice time ADC ramp slope for 160MHz(0) or 80MHZ(1)	0 (160 MHz)
307	Pw_OTA_output_EN	Enable OTAs for charge outputs for all channels	10 (ON)
308	Pw_OTA_output_PP	Force ON or Power pulsing mode (table 5 in § 2.2.3)	
309	Sw_OTA_output	switch off OTA for probe output (0 = OFF, 1=ON)	1 (ON)
310	Pw_Slow_lvds_rcvr_EN	Enable lvds_receivers for Val_event signals	10 (ON)
311	Pw_Slow_lvds_rcvr_PP	Force ON or Power pulsing mode (table 5 in § 2.2.3)	
312	Sw_40MHz_lvds	switch off 40MHZ lvds receiver (0 = OFF, 1=ON)	1 (ON)
313	Sw_160MHz_lvds	switch off 160MHZ lvds receiver (0 = OFF, 1=ON)	1 (ON)

314	sel_clkDiv4	select ext. (0) or int. (1) 40MHz (int = 160MHz/4, ext : LVDS Receiver)	1 (internal)
315	sel_80M	Select readout clock (0= input clk, 1 = input clk/2) but always 80MHZ	1 (160MHz / 2)
316	Dis_ovfCpt	Disable buffer for overflow of Timestamp counter (0 = en, 1 = dis)	1 (disable)
317	sel ext Raz channel	0= internal Raz, 1= external Raz (for debugging)	0 (internal)
318	Not used		
319	sel ext Read	0= internal Read, 1= external Read (for debugging)	0 (internal)
320	EN_TacReadout	Enable readout of Tac data : 0= no Data, 1= data readOut	0 (no data)
321	EN_NOR16	Enable output buffer for NOR16 : 0= disable, 1= enable	1 (enable readout)
322	EN_transmit	Enable output buffers for transmit on : 0= dis., 1= enable	1 (enable readout)
323	EN_data_oc	Enable output buffers for data readout : 0= dis., 1= enable	1 (enable readout)
324	Dis_trigger	disable buffers for triggers : 0 = enable, 1 = disable	0 (enable trig)
325	Pw_lvds_transmitter_EN	Enable LVDS transmitters for DATA output	10 (ON)
326	Pw_lvds_transmitter_PP	Force ON or Power pulsing mode (table 5 in § 2.2.3)	
327	Sw_1mA_TX	Increase bias current in data transmitter (+1mA and + 2mA) 0 =OFF, 1= ON	11 +1mA+2mA
328	Sw_2mA_TX		

2.2.2 Probe register

A probe register is integrated for debugging internal signals. The output of the analog probe is available on pin 91 and the outputs of the 2 digital probes are available on the pins 98 and 99. Only one signal can be observed in each probe (listed in table 4).

This probe register works in the same way as the slow control (SC) register described previously. It shares the same input (sr_in on pin 168), output (sr_out on pin 157), reset (sr_rstb on pin 165) and clock (sr_clk on pin 162) as the slow control register. The "select" signal (pin 160) allows choosing the register to be used. When select is set to "1", the slow control register is used and when select is set to "0", the probe register is used.

Table 4 Probe register parameters

32	Charge and time ADC input signals for channel 0 to 15	0	A_probe
32	ReadSCA0 and RazChnb for channel 0 to 15	32	D_probe2 + D_probe1 (note1)
16	fast shaper output for channel 0 to 15	64	A_probe
48	THb_SCA0_Q, THb_SCA1_Q, ValGain for channel 0 to 15	80	D_probe1 + D_probe2 + D_probe2 (note1)
32	Slow shaper HG + slow shaper LG outputs for channel 0 to 15	128	A_probe
32	preamp HG + preamp LG outputs for channel 0 to 15	160	A_probe
1	LoadValGain	192	D_probe2
1	StartAdcRampb	193	D_probe1
		194	

A_probe= Analog probe (pin 91)
D_probe1= 1st digital probe (pin 98)
D_probe2= 2nd digital probe (pin 99)

note 1 :
ReadSCA0<i> → D_probe2
RazChnb<i> → D_probe1
THb-SCA0_Q<i> → D_probe1
Tb_SCA1_Q<i> → D_probe2
ValGain<i> → D_probe2

2.2.3 Power Pulsing

Each unused stage can be disabled to reduce power consumption. This is controlled by the slow control bits called “EN_bloc-name” or “Pw_bloc-name_EN” (EN= enable). Moreover, each chip stage can be switched off dynamically thanks to the “power_on” command (pwr_on provided by pin 104). This mode is the power pulsing function (see figure 5): for each stage, the slow control bit called “Pw_bloc-name_PP” (PP=Power Pulsing) allows bypassing this feature by forcing it ON. (Refer to the truth table 5 below).

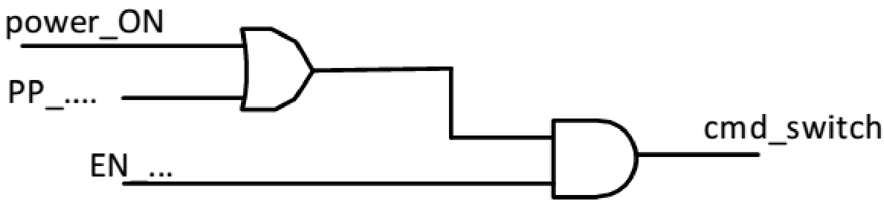

Figure 5 Power pulsing control logic

Table 5 Power pulsing truth table

En_... parameter	PP_... parameter	Power_ON pin	Cmd_switch Internal net	Comments
0	X	X	0	Stage disabled – Forced OFF
1	1	X	1	Stage powered – Forced ON
1	0	1 / 0	1 / 0	Power pulsing mode

2.3 ASIC I/O connections

2.3.1 Front-end connections

The signal input pins, in<0:15>, are available on even pins from 8 to 38. As the preamplifier is a voltage amplifier, a 50 ohm resistor must be integrated on the board for each channel, externally to the ASIC, to adapt the input cable impedance.

2.3.2 Backend connections

The 16 trigger outputs are available on pins 125 to 132 for Tb<15:8> and 135 to 142 for Tb<7:0>. The output corresponds to the direct discriminator output through an internal buffer whose VH supply could be set at CMOS (VH=3.3V) or custom CMOS (2.5V or 1.8V) level (No external component is necessary).VL is set to ground. The triggers are active low.

The NOR16 signal is an analog “NOR” of the 16 discriminator outputs and is active low as soon as one of the 16 discriminators fires. This signal is available on pin 166. It is outputted through an open collector buffer with 200K resistor connected internally to the power supply (3.3V). The user can add a smaller resistor (down to 50 Ohm) outside the chip and connected to VH or 3.3V, if needed to adapt the output cable or speed up the signal.

The Charge and Time measurements for each channel are coded in Gray internally over 10 bits. These coded data are sent in 2 serial links, each one for 8 channels (Dout1 for channels

0 to 7 and Dout2 for channels 8 to 15)). These 2 data outputs are available in both LVDS or Open Collector mode (on pins 144-145 for Dout1 in LVDS mode, on pins 146-147 for Dout2 in LVDS mode, on pin 148 for Dout1 in Open Collector mode and on pin 149 for Dout2 in Open collector mode). Open collector mode outputs go out thru a buffer but without internal resistor, an external resistor (100 Ohm) must be added between the output pin and the custom CMOS power supply (VH) if this mode is used. For fast applications, using the LVDS data outputs is better, and a 100 ohms termination resistor must be added externally between the differential lines.

During the transmission of the coded data, a “transmit_on” signal is generated by the chip. Two “transmit_on” signals are available on pins 150 and 151 for respectively Dout1 and Dout2. There are outputted thru an open collector buffer so an external resistor (100 Ohms) must be added between each pin and the VH supply.

The output of the analog probe is available on pin 91. Depending on the probe register (See Table 4), the output of each of the 16 preamplifiers as well as the slow shaper, the fast shaper, the charge analog values, the time analog values can be seen and checked for debug purpose.

The outputs of the 2 digital probes are available on pins 98 and 99. Depending on the probe register (See Table 4), the following signals can be seen and checked for debug purpose:

- on Digital Probe1 output :
  - the reset of each channel (RazChnb)
  - the hold signal on the 1st capacitance of the analog memory (Thb_SCA0_Q) of each channel
  - the global start signal for the ADC ramp (StartADCRAmpb)
- on Digital Probe2 output :
  - the read signal on the analog memory (Read_SCA0) of each channel.
  - the hold signal on the 2nd capacitance of the analog memory (Thb_SCA1_Q) of each channel.
  - the output of gain discriminator (ValGain) for each channel
  - the global signal generated by the acquisition to store the gain value in all channels (LoadValGain)

2.3.3 Supplies, references, biases

As shown in the Table 2 describing the pinout of the ASIC, there is specific power supply for each block, called vdd_cellname. The power supplies are separated inside the chip to avoid couplings. However, all the power supplies can be gathered and connected to a common vdd=3.3V (each one decoupled with 100nF) except for vdda_pa (pins 9, 21 and 35) which must be connected to a specific vdda=3.3V well filtered with a RC filter (1Ohm, 10µF) and with 100nF on each pin) and except for the power supplies of the digital blocks (vddd on pins 110 and 152 and vddd2 on pin 124) which can be connected together to a specific vddd=3.3V (with a 100nF decoupling capacitor on each pin).

The power supplies VH and VL are used for the digital output buffers. They could be used CMOS level but they could be reduced to provide a low voltage level called custom CMOS. VH can be set from 3.3V (vddd) down to 1.8V (custom CMOS). VL can be set to ground.

All the ground pins (gnd_cell and vss) can be connected together to the general ground of the board.

The bias voltages (ib_cell) and reference voltages (vref_...) are generated internally and are available on pins only for measurement or adjustment. Their values are given in Table2. No external component is necessary on these points (except for the pins listed in Table2) except decoupling capacitances (100nF). All the reference voltages are provided by a common internal bandgap.

3 ASIC description

3.1 Preamplifier

Two voltage preamplifiers with variable gain have been designed in each channel to split the input dynamic range in two parts. The utility of this separation comes from the requirement of a large dynamic range and then to preserve a good charge precision. The low and high gain preamplifiers have an input capacitance with fixed value respectively of 5pF and 0.5pF. Moreover, they have a variable feedback capacitance (on 8 bits) adjustable by slow control parameters (see table 3) with default value of 0.25pF. This variable feedback capacitance allows adjusting the gain channel by channel in order to compensate the photomultiplier (PMT) gain variation. Therefore the two preamplifiers have a gain ratio of 10. The voltage reference of the preamplifiers (pin 29= 1 V) is provided by a common internal bandgap.

The amplified signal feeds two channels: the slow one and the fast one (described later).

3.2 Fast Channel

The CATIROC ASIC is a self-triggered device, meaning that the chip can be autonomous and decide when to convert charge and time. As such, it requires circuitry that senses whether a pulse exceeds a threshold: the fast channel has been designed for this purpose. This fast channel is made by a fast shaper followed by a discriminator.

The fast shaper is a CRRC filter with a time constant of 5 ns. Its high gain allows to send big signal to the discriminator and thus to trigger easily on 50 fC (1/3 of photoelectron for a PMT with a gain of 10^6). The noise affects not only the resolution of the amplitude measurement but it also determines the minimum signal threshold. In fact, without input signal, the noise will be superimposed on the baseline and same fraction of the noise pulses will cross the discriminator threshold inducing a trigger. The purpose of the fast shaper is to filter the noise and to generate a high fast signal at the discriminator input.

This discriminator is a low offset comparator with threshold settled by an internal 10-bit DAC and common for all channels. When the output of the fast shaper (negative signal) is higher than the threshold of the discriminator (vth_trigger on pin 65), a negative pulse is generated at the output of the discriminator. A slow control parameter (Mask_trigger_discri_ch<0:15> : bits 229 to 244 in table 3) is available for each channel (figure 6) in order to disable the trigger. When the bit is set to 1, the trigger output is disabling. An external input, named “trig_ext” (pin 163), is available to inject an external trigger or to make a “veto” of the internal one.

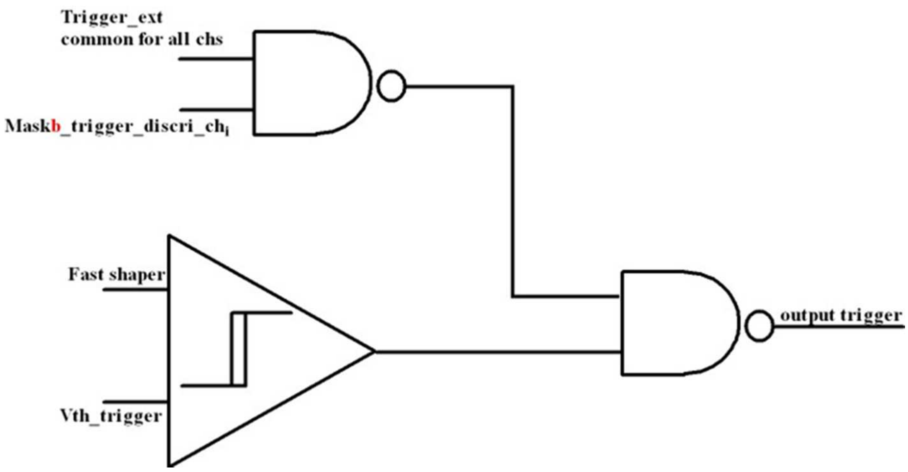

Figure 6 Mask and external trigger schematic

The 16 triggers (pins 125 to132 and 135 to 142) go out thru buffers, the power supply of which can be tuned at 3.3V, 2.5V or 1.8V by changing VH value on test board.

A NOR16 signal (pin 166) is generated as soon as one of the 16 discriminators fires.

For charge measurement, the discriminator output is followed by a variable delay cell in order to hold the charge signal at the maximum of slow shaper output signal. The delay is variable by an 8bit DAC with a minimum value of 5 ns and a linear variation around 1.1ns per DAC unit. The DAC value can be set thanks to the slow control parameters (see table 3: bits 221 to 228).

For time measurement, the discriminator output is followed by a system that manages the start and stop of the TAC Ramp which lasts 25ns.

3.3 Charge channel

The slow channel is made by two slow shapers in parallel dedicated to the high and low gain preamplifiers. The slow shaper is a typical CRRC2 made in two stages (figure 7) with variable gain and peaking time. The peaking time, common for all channels, can vary from 25 ns to 100 ns (Default value: tp= 40 ns; RC= tp/0.574= 70 ns). The gain can change by a feedback variable resistance to compensate the ballistic deficit. The slow shaper configuration parameters are listed in Table 6.

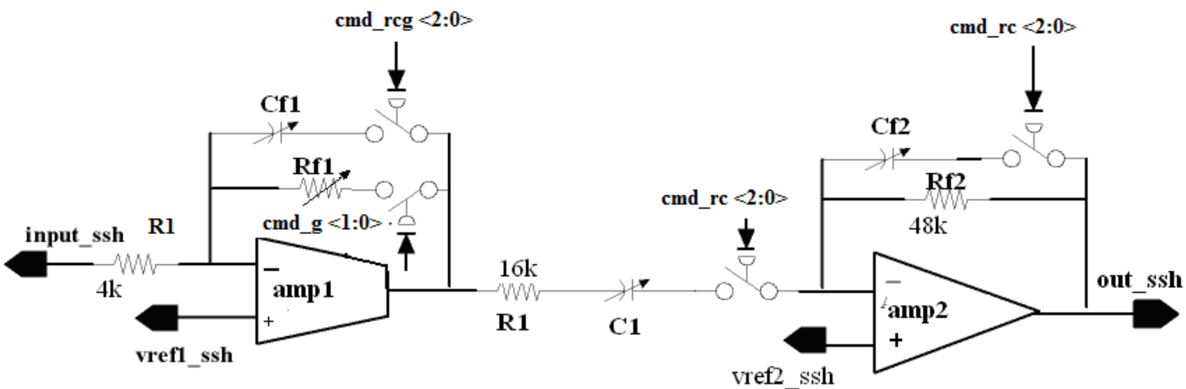

Figure 6 Slow Shaper schematic

Table 6 Slow Shaper parameters.

RC (ns)	Rf1(Ω), Cf1(pF)	Vref1 (V)	Vref2 (V)	R1 (Ω), C1 (pF)	Rf2 (Ω), Cf2 (pF)	Gain
25	16K, 1.5625	1.21	1 V	16K, 1.5625	48K, 0.5208	1
50	16K, 3.125	1.21		16K, 3.125	48K, 1.0416	0.5
	32K, 1.5625	1.12				1
100	16K, 6.25	1.21		16K, 6.25	48K, 2.083	0.25
	64K, 1.5625	1.06				1

	RC 25ns	RC 50ns		RC 100ns	
	G=1	**G=1**	**G=0.5**	**G=1**	**G=0.25**
Cmd_g<1>	1	1	1	0	1
Cmd_g<0>	1	0	1	0	1
Cmd_rc<2>	0	0	0	1	1
Cmd_rc<1>	0	1	1	0	0
Cmd_rc<0>	1	0	0	0	0
Cmd_rgc<2>	0	0	0	0	1
Cmd_rgc<1>	0	0	1	0	0
Cmd_rgc<0>	1	1	0	1	0

The two outputs of the shapers are sent in two analog memories (SCA: Switched Capacitor Array) (figure 8). Each one made by two T&H with a capacitor of 500fF to store the analog charge.

The hold signal allows storing the maximum of the slow shaper signal in the SCA. This signal is generated by the discriminator output delayed by a variable delay box (Slow control bits: 221 to 228) in table3 (figure 9 to 11).

The two T&H work in a "ping-pong mode": while the first value is digitized, a second slow shaper signal can be stored in the second capacitor. The HG T&H is followed by a "charge discriminator". It compares the slow shaper HG maximum voltage value with a threshold (Charge threshold on figure 8) which is set by an internal 10-bit DAC common for the 16 channels (Vth_gain on pin 62). When the HG signal is saturated, the LG one is selected. One of these charge analog values is then converted by the internal 10-bit Wilkinson ADC operated at 160 MHz.

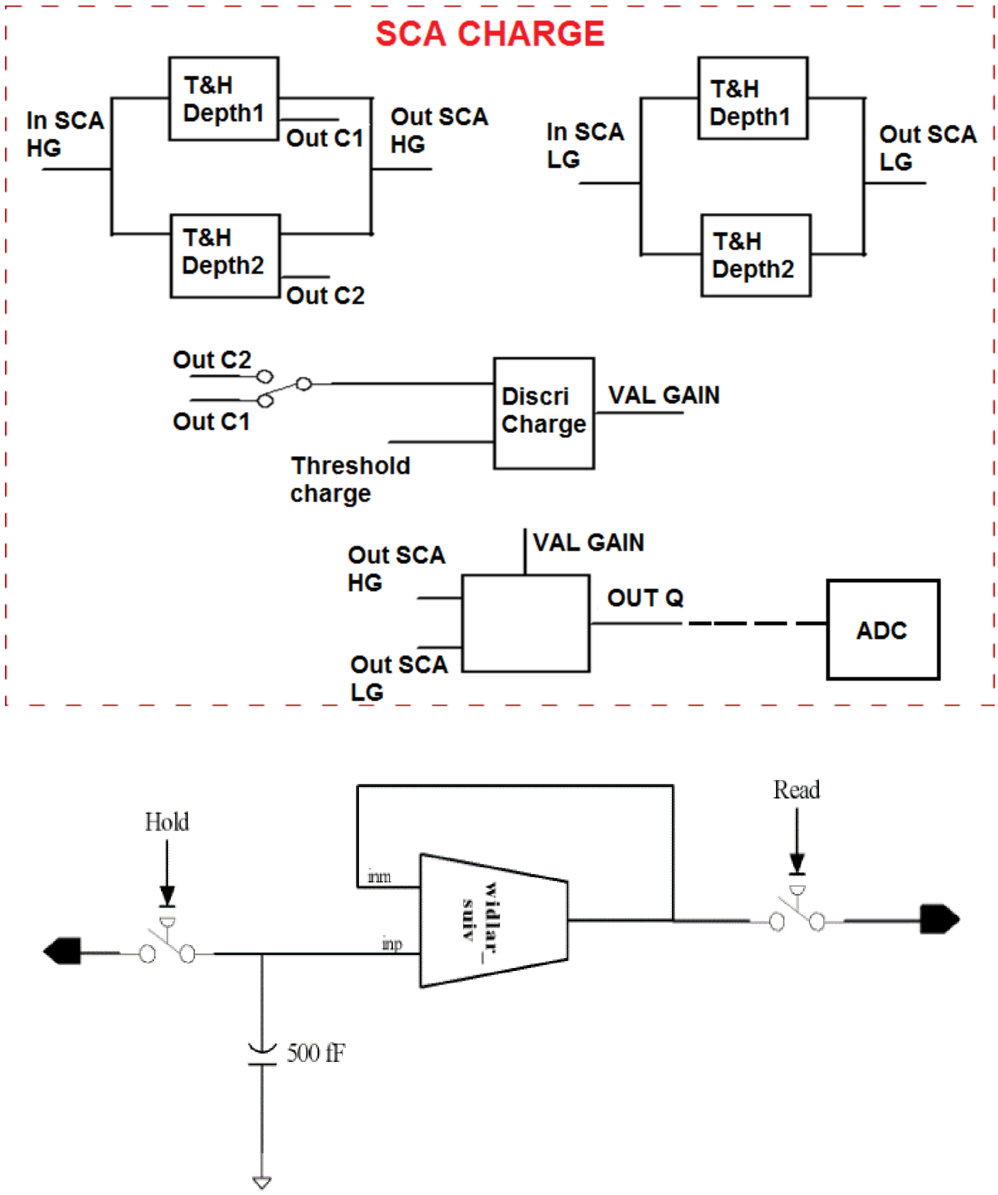

Figure 7 Analog memory schematic (top) and detailed T&H system (bottom)

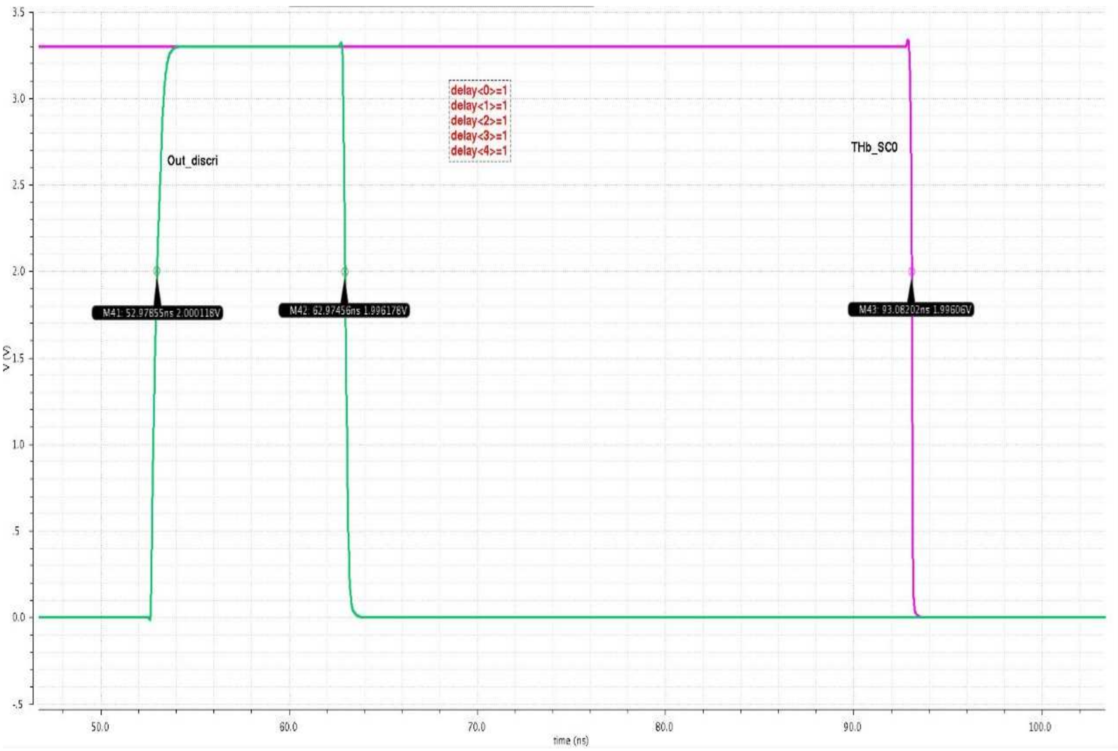

Figure 8 Output trigger and trigger delayed at the slow shaper maximum. (Slow shaper in default configuration).

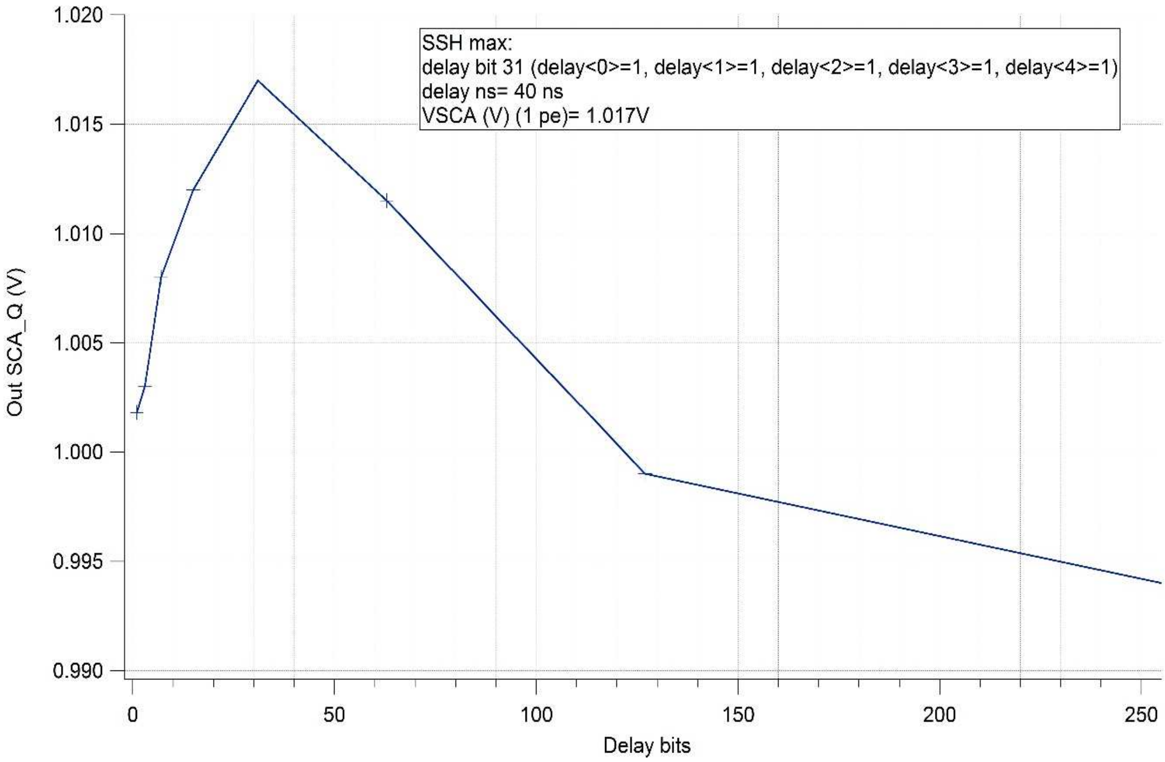

Figure 9 Value of the slow shaper hold signal vs delay. Optimum at delay= 31 (40 ns). Slow control bits: 221 to 228 in table3.

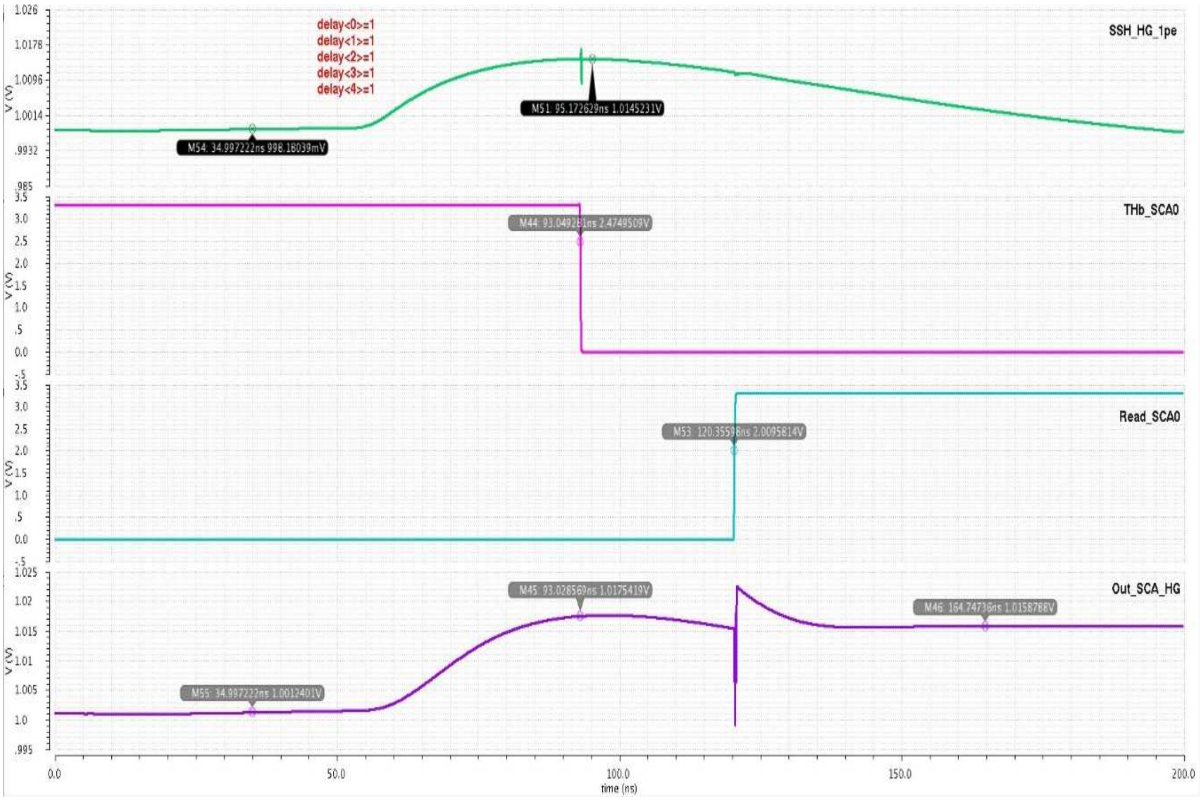

Figure 10 Shaper output signal for 1pe (SSH), trigger signal delayed to shaper maximum (Thb), Read_SCA and SCA output signal (OUT_SCA_HG). Slow shaper in default configuration.

3.4 Time structure

The time measurement is a crucial feature of the ASIC. The ASIC provides the signal “time of arrival” operating in self-triggered mode. In CATIROC, the time measurement is composed of two values:

The “coarse time” (Timestamp) is performed by a 26-bit Gray Counter with a resolution of 25 ns (clock at 40 MHz) and overflows of 1.67 s. An external signal (StartSyst on pin 112) starts the counter. This time is saved in a 26-bit register when the channel has a trigger indicating a detected signal.

The “fine” time based on two TAC ramps in each channel. Inside the 25 ns of the coarse time window, the TAC ramp allows to indicate precisely the time value: the “fine time”. The trigger signal starts the TAC ramp and an internal signal synchronized with the 160 MHz clock and the 40 MHz clock stops the ramp (figure 12). The maximum value of this ramp is saved in an analog memory and converted by a 10-bit ADC. A TAC ramp is implemented in each channel.

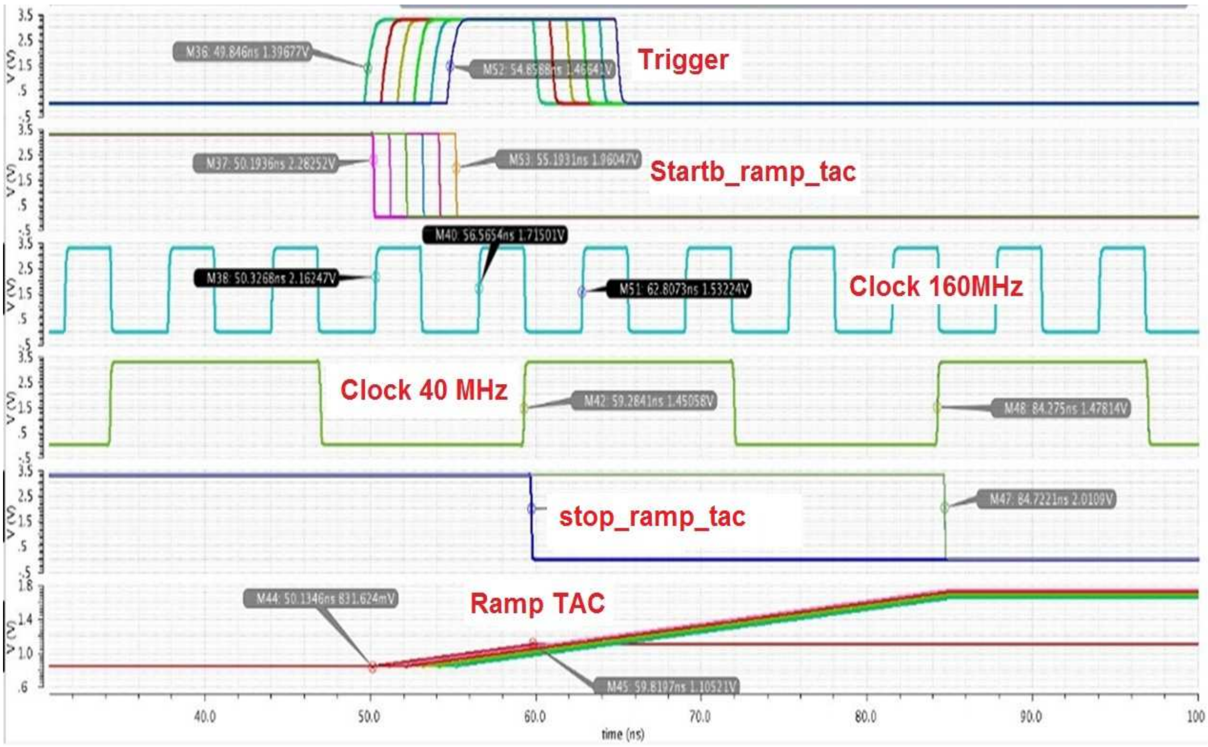

Figure 11 Trigger signal channel0 (at 1pe), Startb_ramp_TAC, Clock_160 MHz, Clock_40 MHz, Stopb_ramp_TAC, RAMP TAC.

The time is given by a combination of the coarse and fine values. The coarse time is the counter value multiplied by the clock step (25ns) and the fine value is obtained by the ADC conversion of the final ramp value.

Time calculation is given by: Ttot= Cpt (Time Stamp)*25ns – (Fine time) where the fine time is: Fine Time= (ADC_{count})*LSB(s)

3.5 Analog to Digital conversion

For data storage and subsequent analysis the analog signals must be digitized. An internal Wilkinson ADC is implemented to convert the analog signals:

- The charge value stored in analog memory with depth of 2 (SCA)
- The fine time value as the final value of the two TAC ramps

In each channel, 2 discriminators with a common ramp as reference (two ramps are implemented, one for charge and a second for time measurements) are used to compare and to convert the data.

When one or more channels are hit, the trigger signal indicates to the digital part that the SCA cell is full and so the hit channels are loaded and the conversion is started. The “start ramp ADC” signal is sent to the ADC ramp and the 160 MHz counter (10-bit Gray Counter) is started. When the charge and the time of all the 16 channels are converted (stored in the registers) the digital part stops the conversion and then starts the readout of the data.

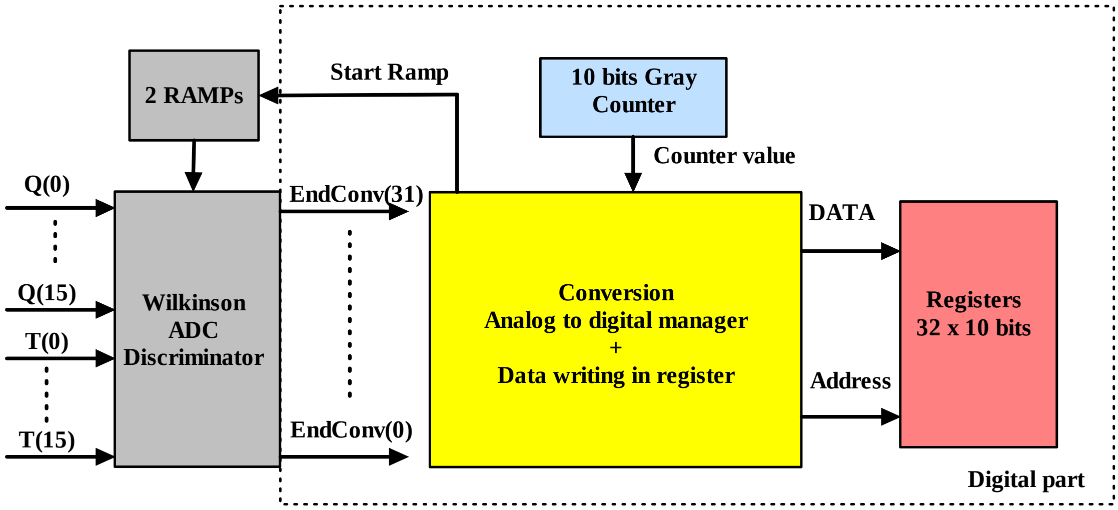

Figure 12 Conversion module

3.6 Digital read-out

The digital part manages the coarse time tagging, the internal ADC and the readout process. To perform these tasks, it requires two global clocks, a 40 MHz clock ("ck_40" on pins 120-121) and a 160 MHz clock ("ck_160" on pins 117-118) and a global reset (Resetb on pin 111) to be set at '1'.

The signal StartSyst (pin 112) (to provide externally) starts the digital part. It stats the "time stamp" counter at the same time.

The converted data, outputted on Dout1 and Dout2 (pins 144-145, 146-147, 148 and 149) (see paragraph 2.2 - Backend connections), are valid when the TransmitOnb1 and 2 (pins 150 and 151) are at a '0' logic level.

The digital part of the chip is divided in 2 blocks: 1 block for 8 channels. For each block, we have one serial link to readout the internal memories. The readout is made in 2 frames. Only channels readout in the first frame are readout during the second one. It implies that the number of words sent is equal for the 2 frames.

All the data are encoded in Gray format and the readout process is done MSB and low address first. The data are sent at 80MHz (ck_160 divided by 2 internally).

As an example, a chronogram of the readout frames is given below:

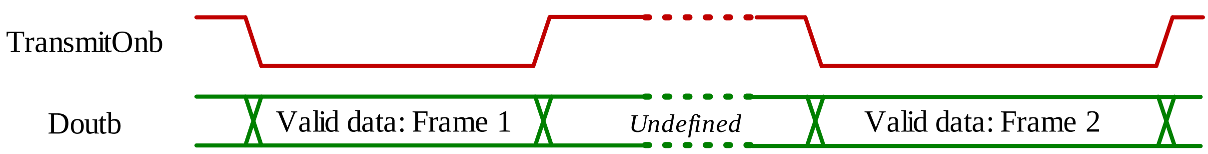

Figure 13 Chronogram of the readout frames

The first frame is composed by a maximum of 8 words of 29 bits populated with:

- 3 bits for channel number
- 26 bits for coarse time counter

The memory mapping of this frame is given below:

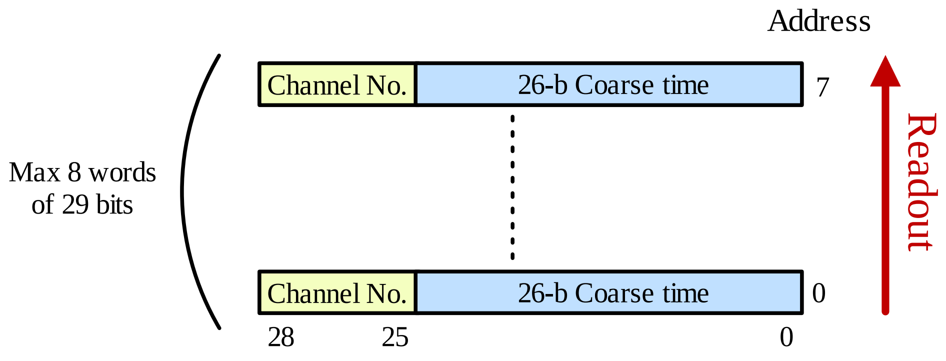

Figure 14 Memory mapping first frame

The second frame is composed by a maximum of 8 words of 21 bits feed by:

- 1 bit for the gain used during conversion (High or Low gain)
- 10 bits for the ADC result of the analog charge
- 10 bits for the ADC result of the fine time

The memory mapping is given hereafter:

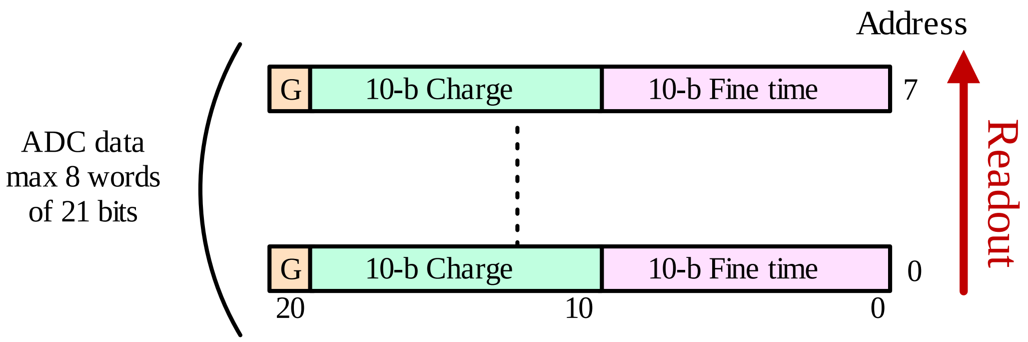

Figure 15 Memory mapping second frame

3.7 Hit Rate

The charge and time analog values are saved in two analog memories (SCA) each with depth of two (see paragraph 3.3). Two capacitances allow to storing the charge and time measurements and are treated in ping-pong mode. When a signal hits one channel, it is stored firstly in the first capacitance. During the conversion, a second signal could be stored in the 2nd capacitance of the memory. The signals of the 16 channels are managed in parallel by the digital part.

The maximum duration of conversion is given by: $Tconv = \frac{2^n}{F_{conv}}$ = 6.4 µs

where: "n" is the number of ADC bits (10) and Fconv is the conversion frequency (160MHz).

The time of read out given by: $TRO = \frac{n° \, of \, channels * number \, of \, bit}{F_{RO}}$

The coded data are sent in parallel in two serial links to be readout (the first link for ch0 to ch7 and the second for ch8 to ch15). The readout is made of 2 frames (see paragraph 3.6 "digital read out"). The first frame (21 bits) is read out during the conversion of the charge and the time (2^{nd} frame). The read out time is then given only by the second frame (29 bits). With the read out frequency at 80 MHz, the maximum read out time is 3 µs (when all the channels (8) are hit)

$$TRO = \frac{8 * 29}{80 \, MHz} = 3 \, \mu s$$

This time depends on the number of hit channels (n): the read out of each channel takes 0.36 µs

The maximum time to treat (convert and read out) the signal is given by:

Tcycle= Tconv+TRO= 6.4 µs+3 µs= 9.4 µs

During these 9.4 µs, if a second signal arrives, it is saved in the second capacitance of the SCA.

The second signal can be shaped by the slow shaper after 500 ns (for RC= 100 ns) to avoid the slow shaper output signals pileup. In the same channel, a third signal could be saved again in the first capacitance of the analog memory after 9.4 µs. So the hit rate frequency for each channel is around 100 KHz (1/9.4µs). This rate is the lower one (calculated in worst case) and will be increase if the number of hit channels is less than 100 %.

Table 7 Hit rate

HIT RATE			
Tconv (1 ch)	6.4 µs	Tconv (16 ch)	6.4 µs
Tread-out (1 ch)	0.36 µs	Tread-out (16 ch)	3 µs
Tcycle (1 ch)	6.8 µs	Tcycle (16 ch)	9.4 µs
Hit rate (1 ch)	150 kHz	**Hit rate (16 ch)**	100 kHz

4 ASIC performance

The CATIROC die has a surface of 13.2 mm² (3.3 mm × 4 mm) and is packaged in TQFP208. A dedicated testboard (figure 17) is designed to perform the ASIC characterization. It contains a FPGA (Field Programmable Gate Array) which handles the communication with the ASIC, it provides the two differential clocks (40 MHz and 160 MHz) and allows to send slow control parameters and read out the digital data coming out of the chip.

The main part of the firmware inside the FPGA is written in VHDL language and one part of this firmware manages the communication between the ASIC and the PC via a USB connection. The communication between the PC and the board is managed by Labview program.

A dedicated Labview program is developed and it allows to send the ASIC configuration (slow control parameters, probe parameters,..) and to receive the output bits via an USB cable connected to the test board.

16 SMA input connectors or a 64-pin straight connector (16 inputs + 48 gnd) achieve the connection between the input signals and the 16 ASIC inputs. A signal generator is used to create the input charge injected in the ASIC. The input signal, used in measurements, is a pulse signal with 5 ns rise and fall time and 10 ns of duration. This current signal is sent to an external resistor (50 Ohms) placed in the ASIC input on the board. An SMA output connector named "Analog probe" is placed to observe the analog signals on the oscilloscope.

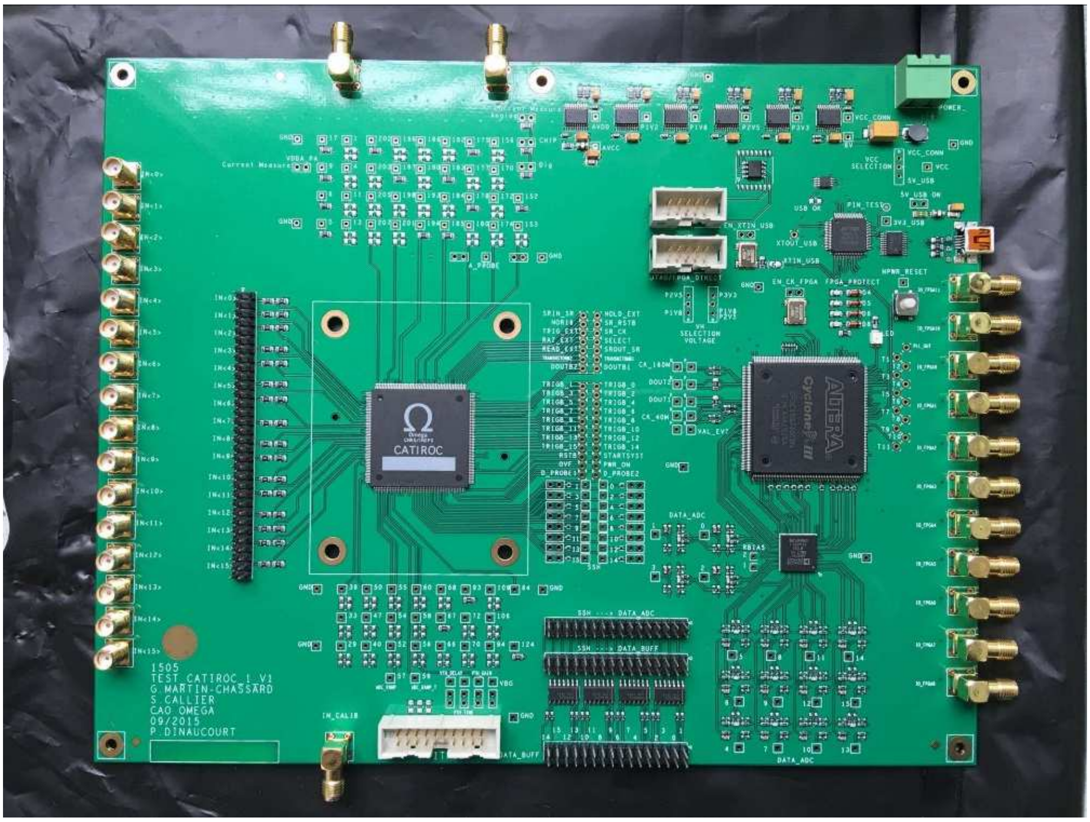

Figure 16 CATIROC Test board.

4.1 Input signal

The input signal is made by a pulse generator signal: a negative voltage pulse (rise time= 5ns, fall time= 5ns, width= 10 ns, Amplitude @1 p.e.~ 0.8 mV). The M.I.P. is 1 p.e.= 160 fC @ PMT gain 10^6.

4.2 General tests

A lot of features have been embedded in the ASIC so the consumption is 21 mW/channel related to a power supply of 3.3 V. Unused parts can be switched off by slow control (paragraph 2.2.3).

The first measurements on the analog blocks (preamplifier, shaper, etc) focused on the study of the analog waveforms. These output waveforms indicate amplitude values comparable to the simulations. Table 9 lists the main performances of the analog blocks: the gain, the noise and the Signal to Noise Ratio (SNR) referred to the single photo-electron (p.e.).

The discrepancies obtained in measurements and simulations, in terms of amplitude and peaking time, are due to the output buffer placed on the test board to observe the analog waveforms on the oscilloscope. In addition, the response of a filter depends directly on the shape of its input signal. This explains the relevant difference measured at the slow and fast shaper outputs.

The analog blocks (preamplifier, shaper, etc) pedestals have a pedestal dispersion of 1.3% around 1V for the preamplifier, 0.5% around 1V for the slow shaper and 0.12% around 1.9 V for fast shaper.

Table 8 Performance of the analog blocks compared in measurement and simulation.

1 p.e. = 160 fC PA: (gain= 20), SSH: (50ns, gain=1)	PA_HG Meas.	PA_HG Sim.	SSH_HG Meas.	SSH_HG Sim.	FSH_HG Meas.	FSH_HG Sim.
Peaking time (ns)	10	5	33	40	7	5
GAIN (mV/p.e.)	10	13.5	15	16	75	97
NOISE (mV)	0.6	0.67	1	1	2.3	3.4
SNR	16.6	20.1	15	16	32	28.5

4.3 10bit-DAC for time and charge thresholds

Two 10-bit DACs are integrated to set two different thresholds: one for the trigger discriminator and the other one for the charge discriminator. The trigger threshold (vth_time) can be set using the SC parameters 278 to 287. The charge discriminator threshold (Vth_gain) can be set using the SC parameters 288 to 297.

The measurement of the linearity of these two DACs (figure 18 and 19) indicates for the trigger DAC a slope of around 800 µV/DAC unit, an intercept of around 1 V and residuals ± 0.05%.

For the charge DAC a slope of around 800 µV/DAC unit, an intercept of around 1 V and residuals ± 0.1%.

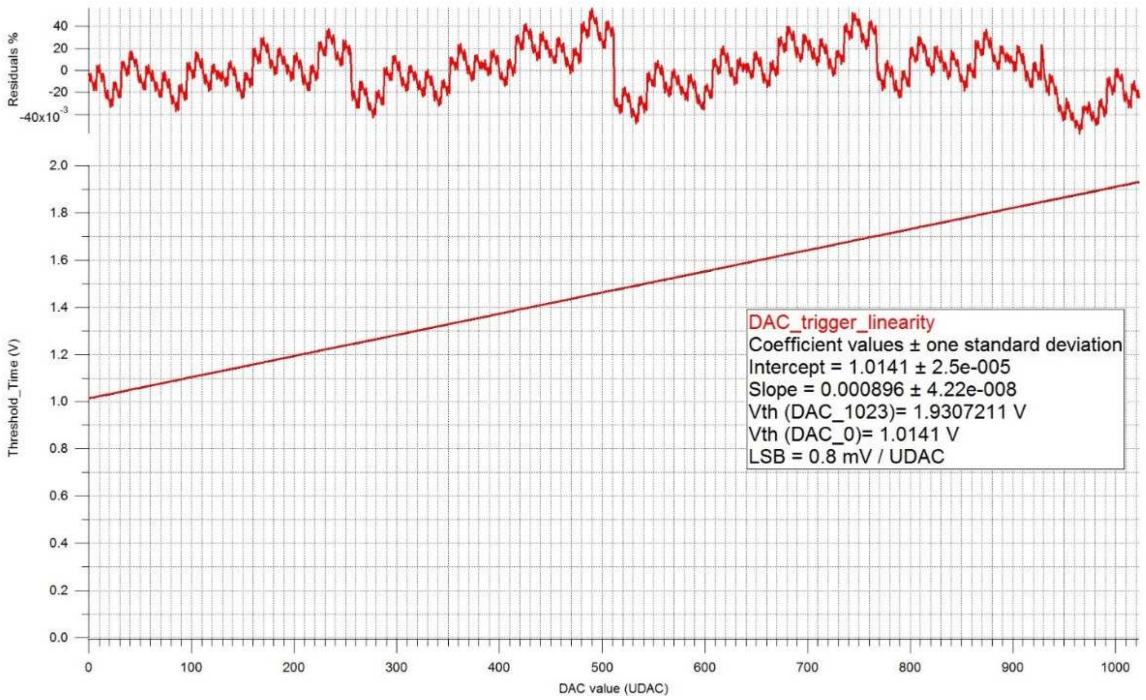

Figure 17 DAC trigger linearity

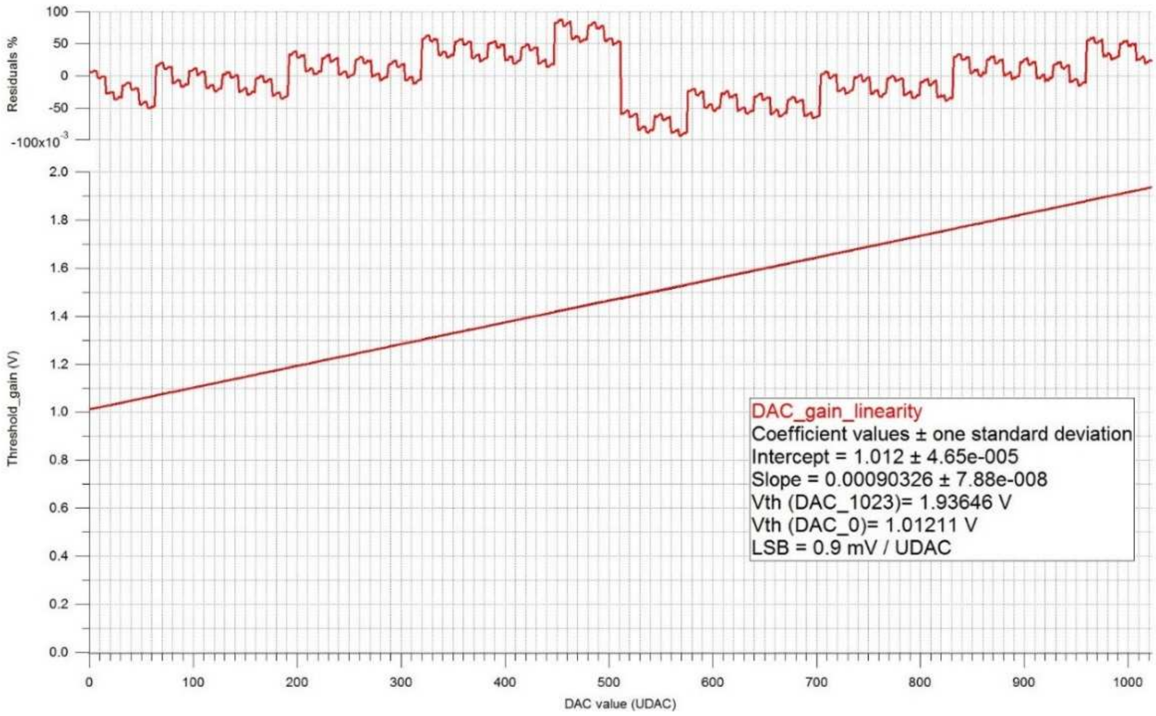

Figure 18 DAC gain linearity

4.4 Trigger efficiency measurements

The trigger efficiency is investigated by the “S-Curve” test: scanning the threshold (Vth_trigger given by an internal DAC and changed by slow control bits n° 278 to 287) for a fixed channel and monitoring the discriminator response. The resulting trigger efficiency is represented as a function of the threshold.

The trigger pedestal is measured without input signal. The figure 20 shows the S-Curve pedestal measurements for the 16 channels: the trigger efficiency versus the threshold in DAC units (1 DACu = 0.8 mV) in two configurations, without the two ASIC clocks (black curves) and with the clocks (red curves). The pedestal mean value is around 967 DACu without clocks and shifts of around 10 DACu to become 975 DACu with clocks.

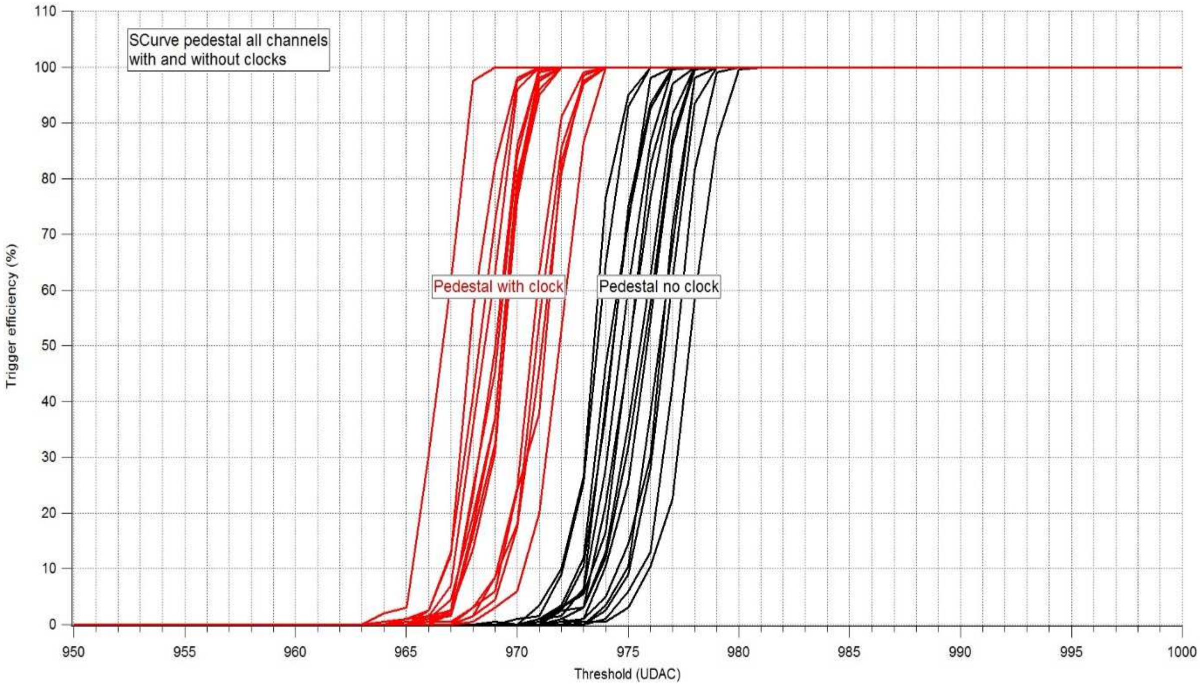

Figure 19 S-Curve pedestal for the 16 channels.

Figure 21 shows the trigger efficiency versus the threshold for different injected charges, from 0 (967 DACu) to 1.4 pC (9 p.e. at 68 DACu). The two curves indicates the test with and without clocks. No threshold shift, due to these clocks, is observed with an input charge. As the fast trigger produces negative pulses, the S-curves are mirrored compared to the usual appearance, with the smallest signals on the right part of the plot.

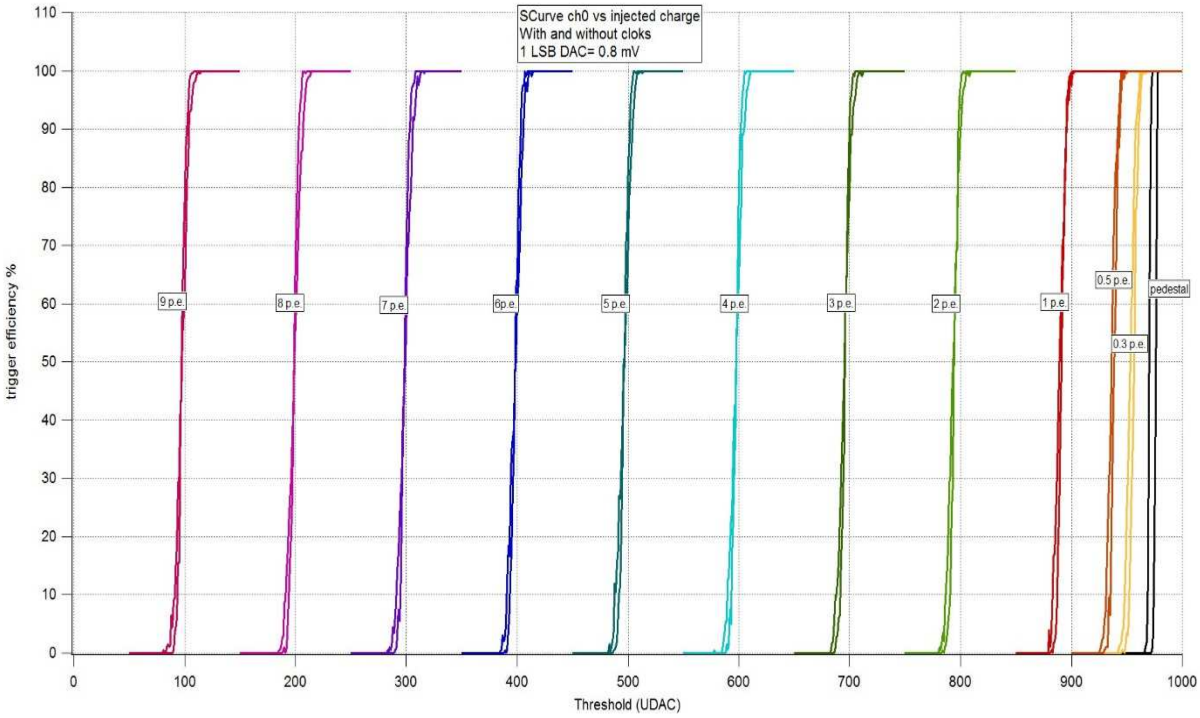

Figure 20 Trigger efficiency vs threshold for various injected charges up to 1.4 pC

The trigger efficiency versus the threshold is tested (without clocks) with various injected charges (up to 800 fC = 5 p.e.) for all the channels (see figure 22). The channels dispersion is around 6 DACu.

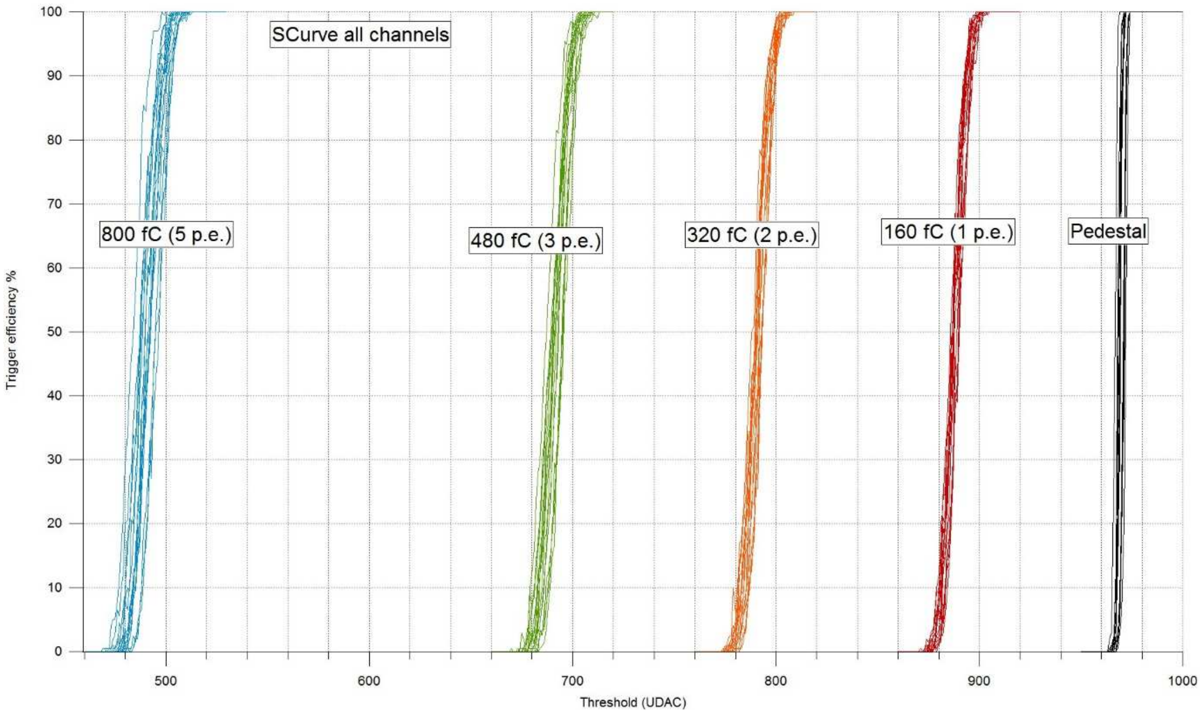

Figure 21 Trigger efficiency vs threshold for various injected charges up to 800 fC (5 p.e.)

The 50% trigger efficiency values extracted from this measurement are plotted, in DAC units, versus the injected charge up to 2 p.e. (figure 23). The plot indicates a sensitivity close to 111.2 DACu/p.e. The noise (figure 24) can also be obtained by fitting the S-curve (at 1 p.e.) and gives a σ equal to 6.31 DACu (corresponding to 9.1 fC). Considering this noise, the signal to noise ratio (SNR) is 17.6. By measure, the minimum threshold is set at 968 DACu (red line on fig. 23).

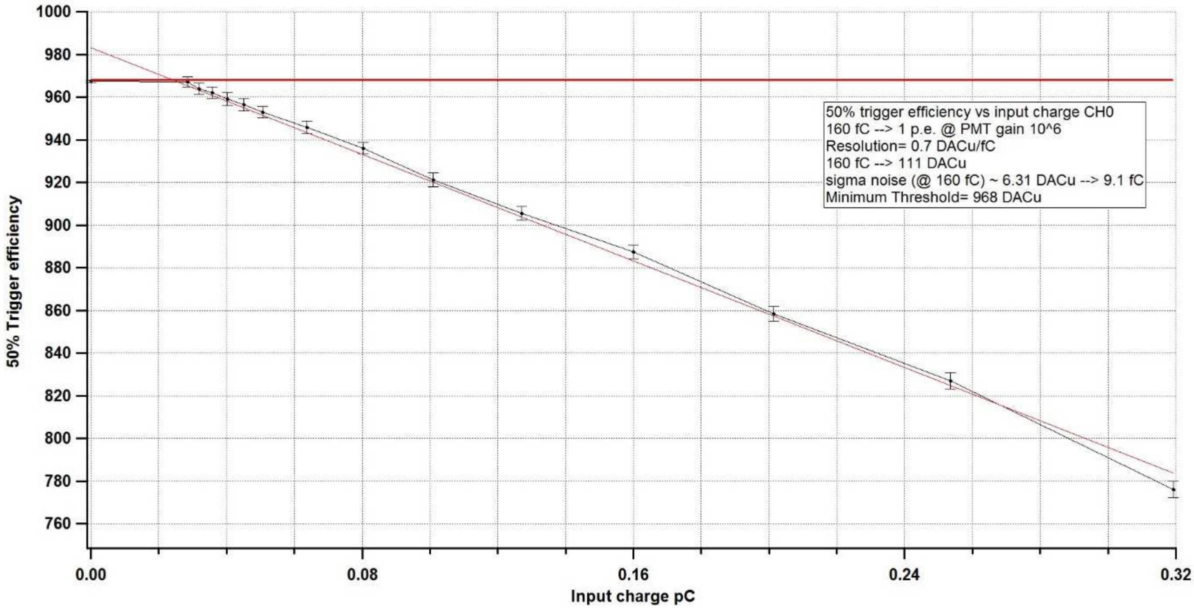

Figure 22. 50 % trigger efficiency versus injected charges.

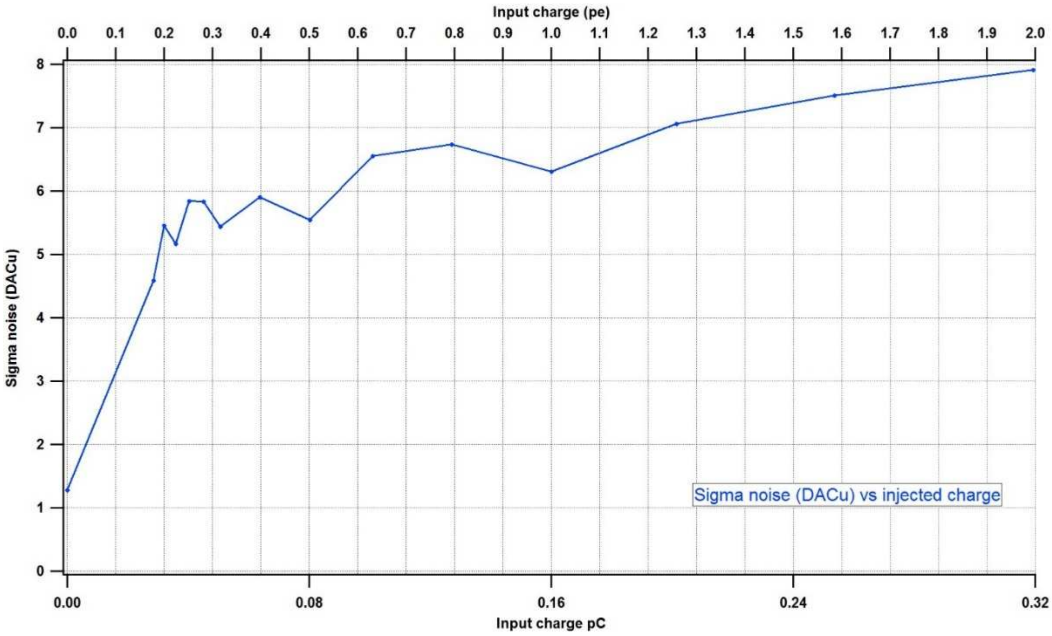

Figure 23 Sigma noise

4.5 Jitter and time walk

Jitter measurements are performed with a threshold set to 1 pe and when the 40MHz and 160MHz clocks are OFF (figure 25). Jitter is around 240 ps at 1 pe and it goes down to 75 ps for charge injection bigger than 8 pe. The 40MHz and 160MHz clocks generate couplings through the substrate and so degrade the jitter performance up to 470 ps at 1 pe and 130 ps for charge injection bigger than 8 pe.

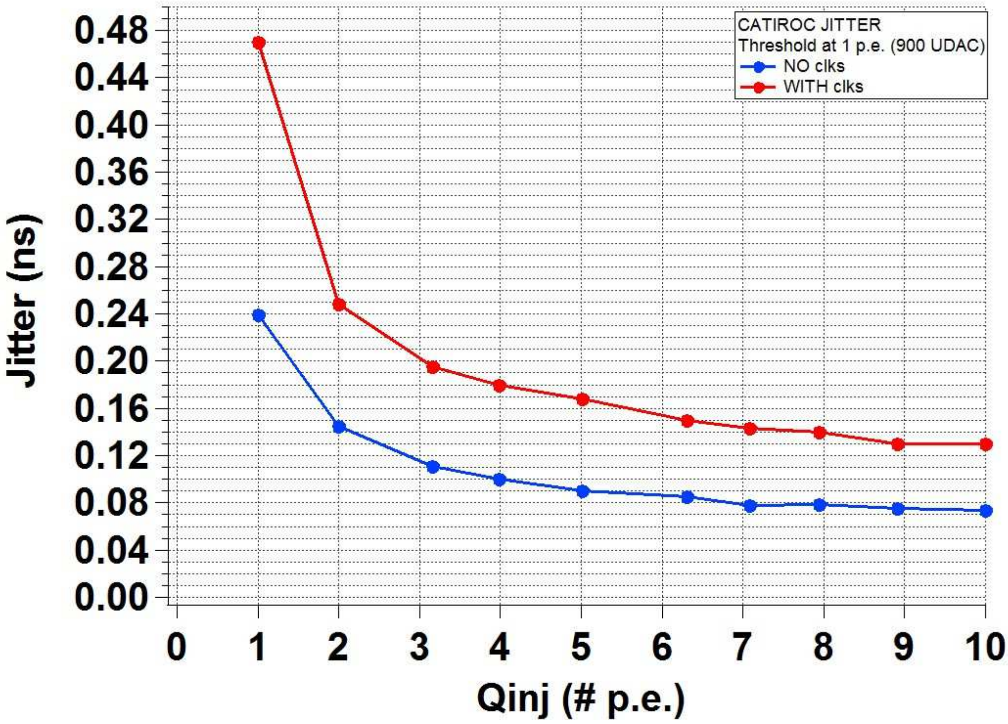

Figure 24 Jitter measurement

In figure 26, time walk is measured from 160 fC (1 pe) to 1.6 pC (10 pe). It is around 5 ns. The test is performed with a threshold at 160fC. The y axis is the time measured between the input signal and the trigger output. In real operation, the trigger time walk of 5 ns needs to be corrected, through the charge measurement available on the internal charge ADC.

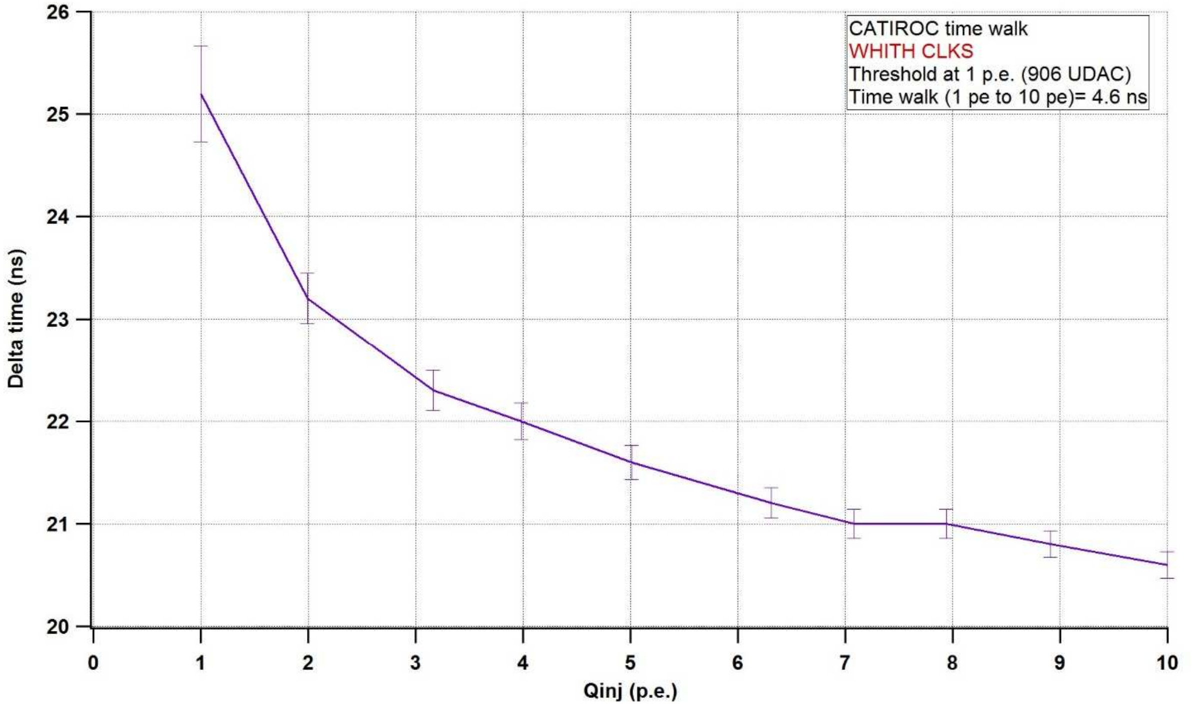

Figure 25 Time walk measurement

4.6 Charge measurement

The charge pedestal is checked at the ADC output without injected charge at the input and with an external trigger. This external trigger is sent by the FPGA in the pin 163 “trig_ext”. In the figure 27 are plotted the charge pedestal mean (red), minimum (green) and maximum (blue) values for every channel.

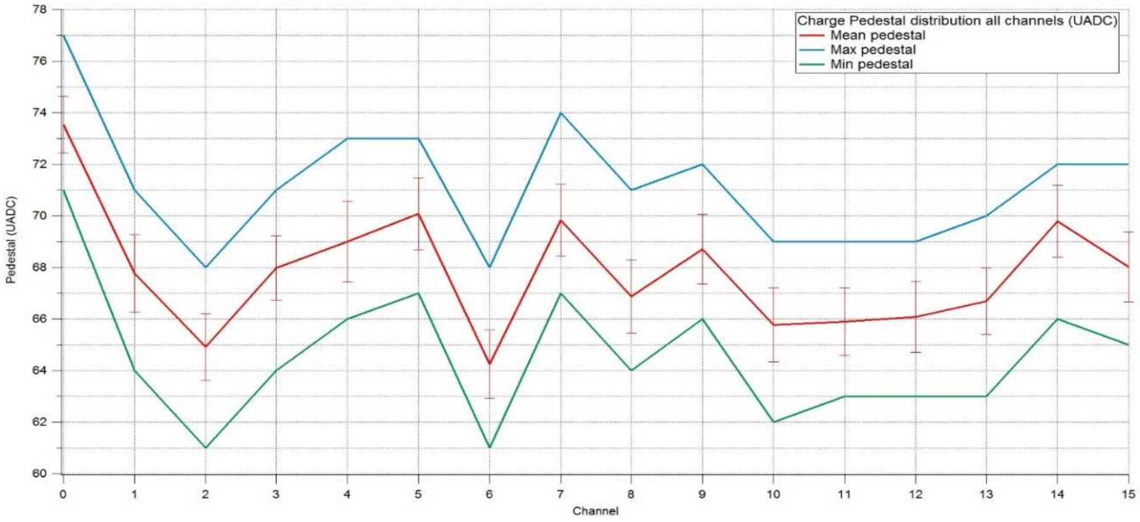

Figure 26 Charge pedestal

The whole chain is tested by injecting known charges at the input of one channel. The signal is amplified, auto-triggered, held in the T&H and converted by the internal ADC. With a shaping time of 50 ns, a slow shaper gain set at 1 and a preamplifier gain at 20, the charge distribution for various input charges (from 1 to 10 p.e.) is shown in figure 28. The sensitivity is 16

ADCu/p.e. and the noise is nicely gaussian with an rms of 1.1 ADCu (0.07 p.e.) (figure 29). This provides a Signal to Noise Ratio (SNR) equal to 14 for the whole chain.

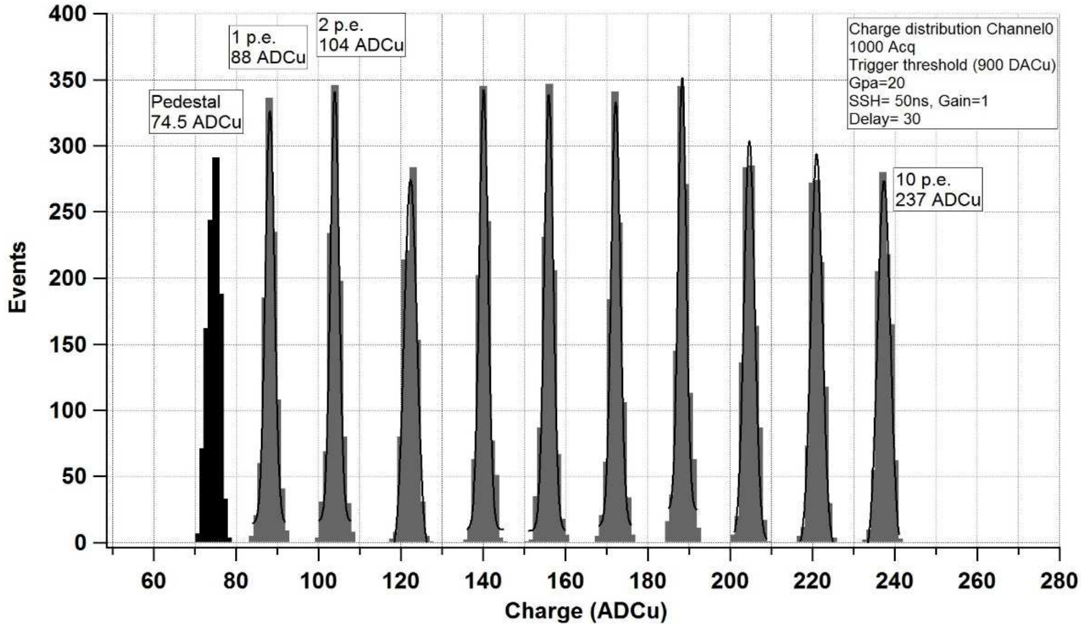

Figure 27 Charge distribution channel 0.

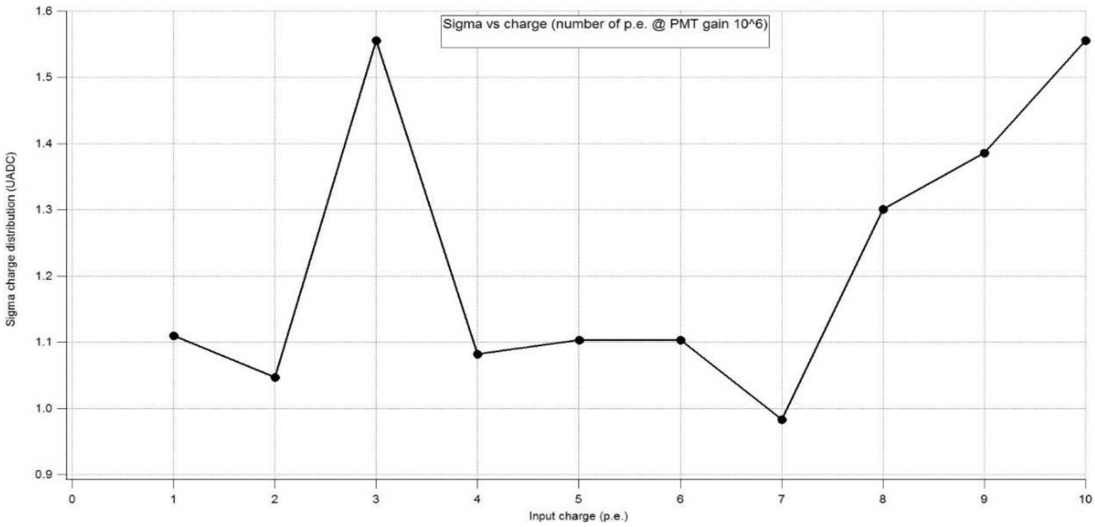

Figure 28 Sigma Gaussian fit of the charge distribution

A charge of 160 fC (1 p.e. @ PMT gain 10^6) is injected in every channels. The measured charge (pedestal subtracted) is plotted in figure 30. The rms value is 15 ADCu.

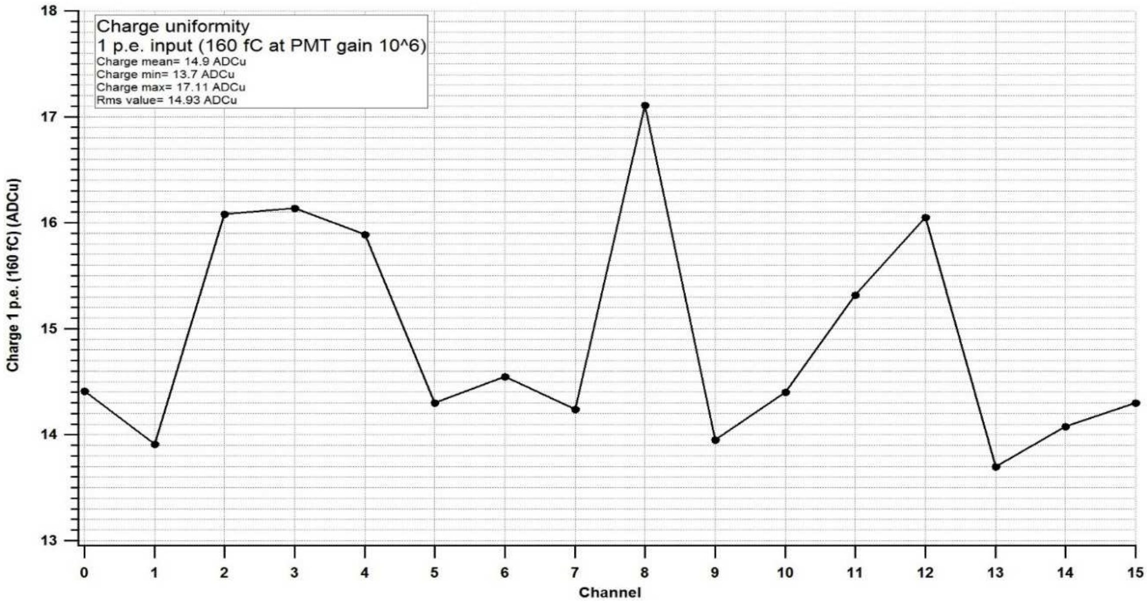

Figure 29. Charge uniformity. 160 fC (1 p.e. @PMT gain 10^6) injected in the 16 channels

The charge linearity on the full dynamic range (using high and low gain path) are measured. As mentioned above, the two analog charges, from the HG and LG path, are saved in the T&H, the non-saturated value is then converted by the internal ADC. The gain selection is possible thanks to the "charge discriminator".

Figure 31 represents the linearity for high gain path (channel 0) at preamplifier gain 20 (black dots) and 10 (blue dots) in forced gain mode (Slow control bit 203 at 0 and bit 246 at 1). The two curves indicate a good dynamic range up to 9 pC (~ 56 p.e.) with residuals better than 0.7 % for gain 20 and up to 15 pC (94 p.e.) with residuals better than 1% for gain 10. The high gain LSB is 10 fC (0.06 p.e.) for gain 20 and 16 fC (0.1 p.e.) for gain 10.

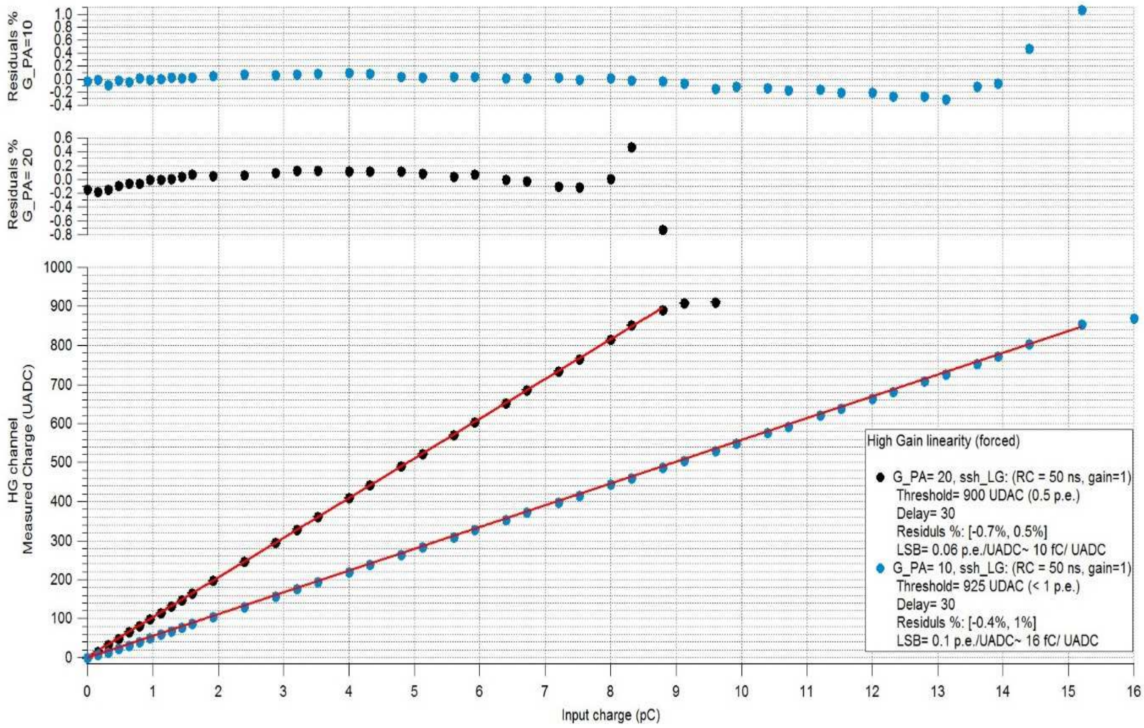

Figure 30 Charge linearity channel 0, HG path for preamplifier gain 20 (black dots) an 10 (blue dots)

Figure 32 represents the linearity for low gain path (channel 0) at preamplifier gain 20 (black dots) and 10 (blue dots) and in forced gain mode (Slow control bit 203 at 0 and bit 246 at 0). The two curves indicate a good dynamic range up to 70 pC (~ 437 p.e.) with residuals better than 0.7 % for gain 20 and up to 120 pC (750 p.e.) with residuals better than 2% for gain 10. The low gain LSB is 80 fC (0.5 p.e.) for gain 20 and 160 fC (1 p.e.) for gain 10.

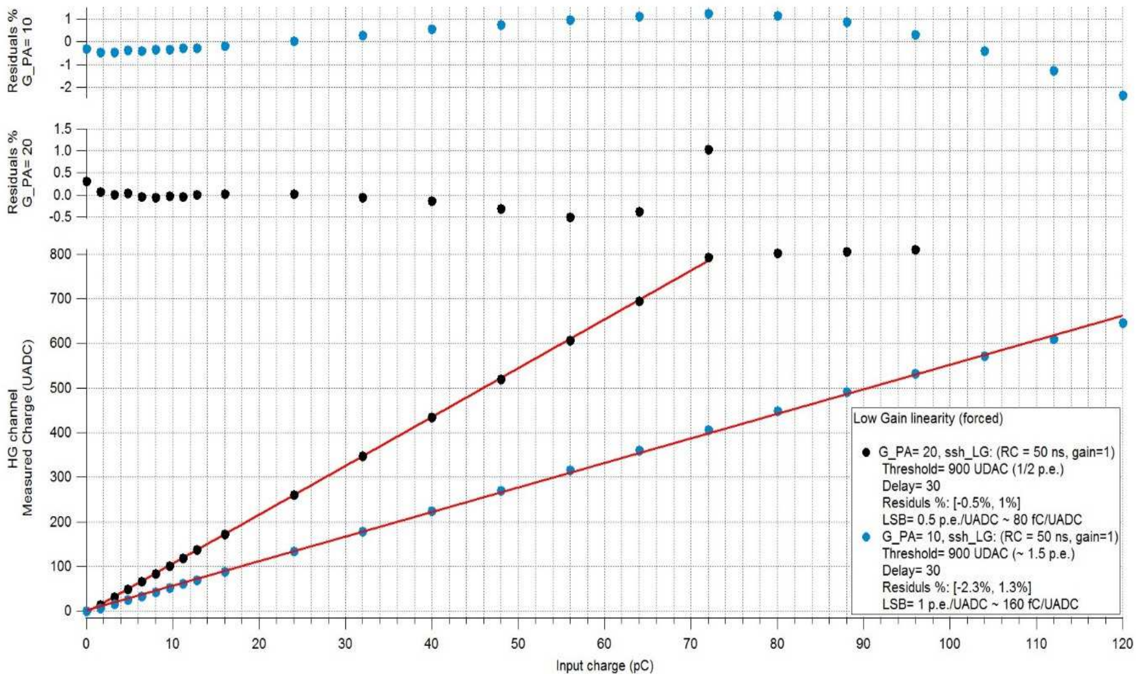

Figure 31 Charge linearity channel 0, LG path for preamplifier gain 20 (black dots) an 10 (blue dots)

Figure 33 illustrates the charge measurements for different injected charges in automatic mode (Slow control bit 203 at 1). The charge threshold (Slow control bit from 289 to 298) is set at 820 DACu (~ 55 p.e.) and the trigger threshold (Slow control bit from 279 to 288) at 900 (~ 80 fC= 0.5 p.e.) for a preamplifier gain at 20. The charge threshold (Slow control bit from 289 to 298) is set at 800 UDAC (~16 pC= 100 p.e.) and the trigger threshold (Slow control bit from 279 to 288) at 900 (~ 80 fC= 1.5 p.e.) for a preamplifier gain at 10.

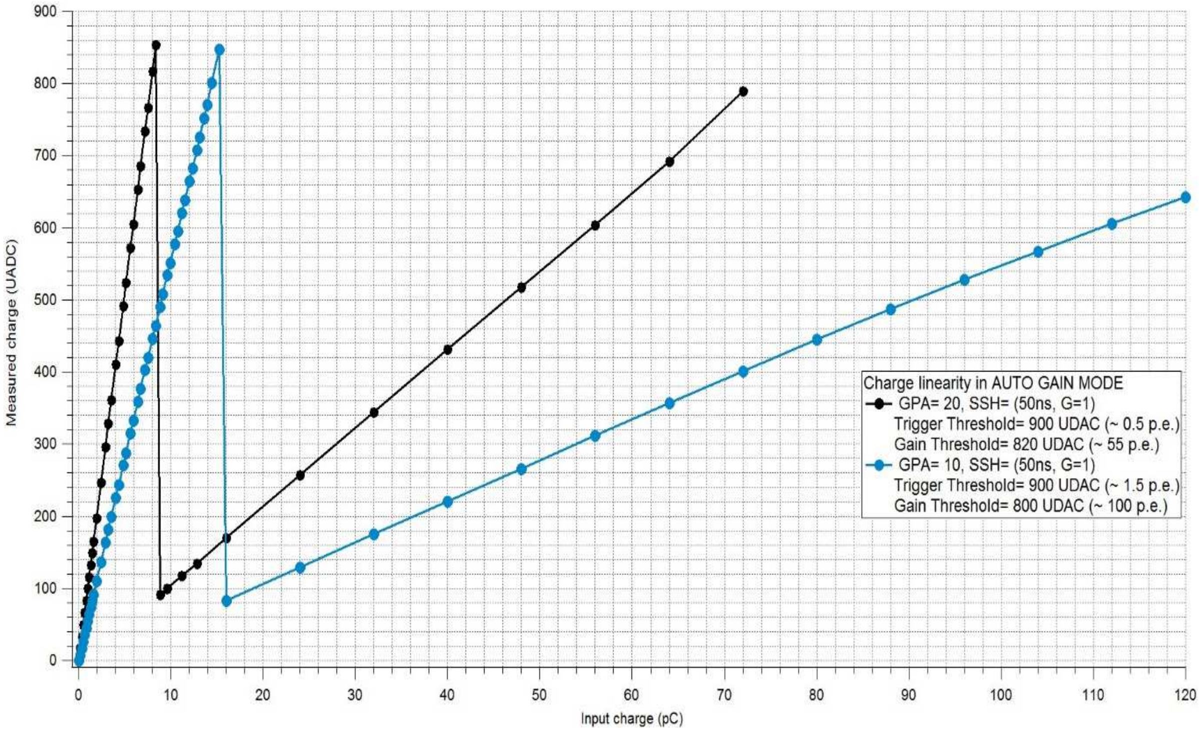

Figure 32 Charge linearity in Auto gain mode

4.7 TAC measurements

The time measurement is a crucial feature of the ASIC. The ASIC provides the signal “time of arrival” operating in self-triggered mode.

The TAC ramp reconstructed is displayed in figure 34. A periodic pulse signal is injected in channel 0 and it is delayed by steps of 100 ps. The linear fit provides the slope which gives a LSB (or ADCu) of: LSB= 1/slope= 27 ps/ADCu (TAC binning). The residuals are within ± 14 ADCu, corresponding to ± 400 ps, with a rms value of 167 ps. The residuals exhibit a periodical shape due to a coupling of the 160 MHz clock, most likely through the substrate. The DNL is less than 1 LSB (figure 35).

Figure 36 indicates the time distribution obtained for an input signal delayed of 5 ns. 1000 acquisitions are measured giving a time distribution where σ = 1.41 ADCu (= 38 ps for an LSB of 27 ps). So the rms value is $\sqrt{167^2+38^2}$= 171 ps.

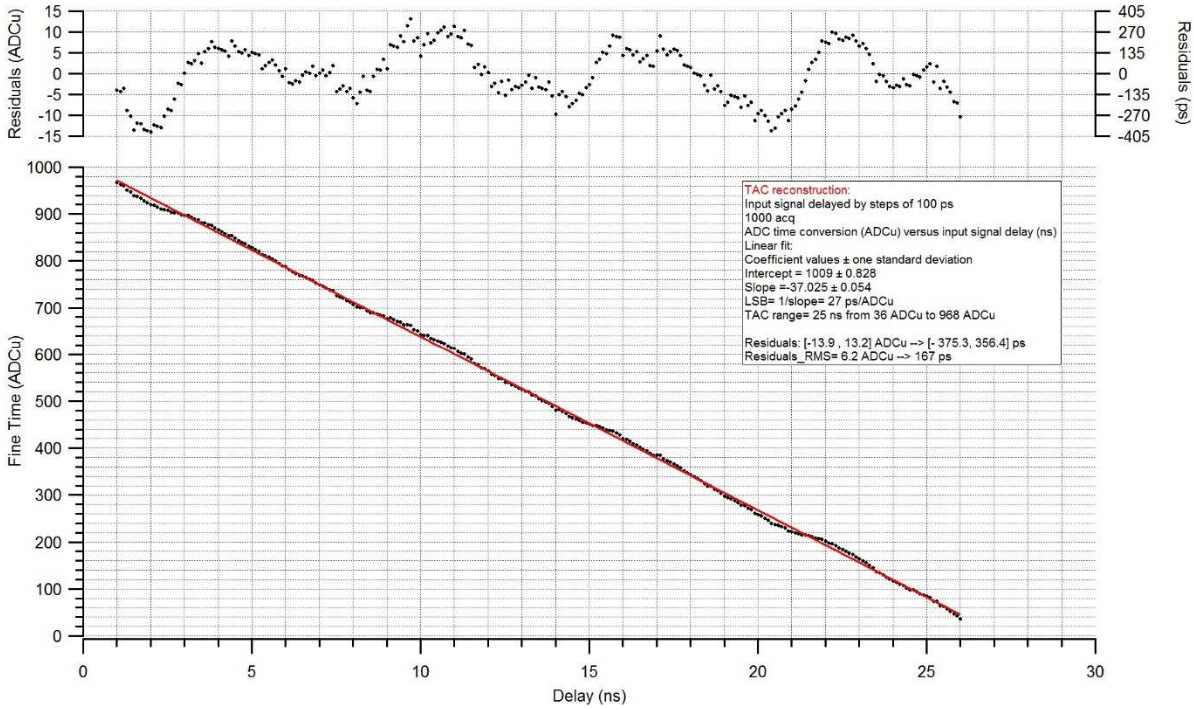

Figure 33 TAC reconstruction with linear fit and TAC INL (ADCu)

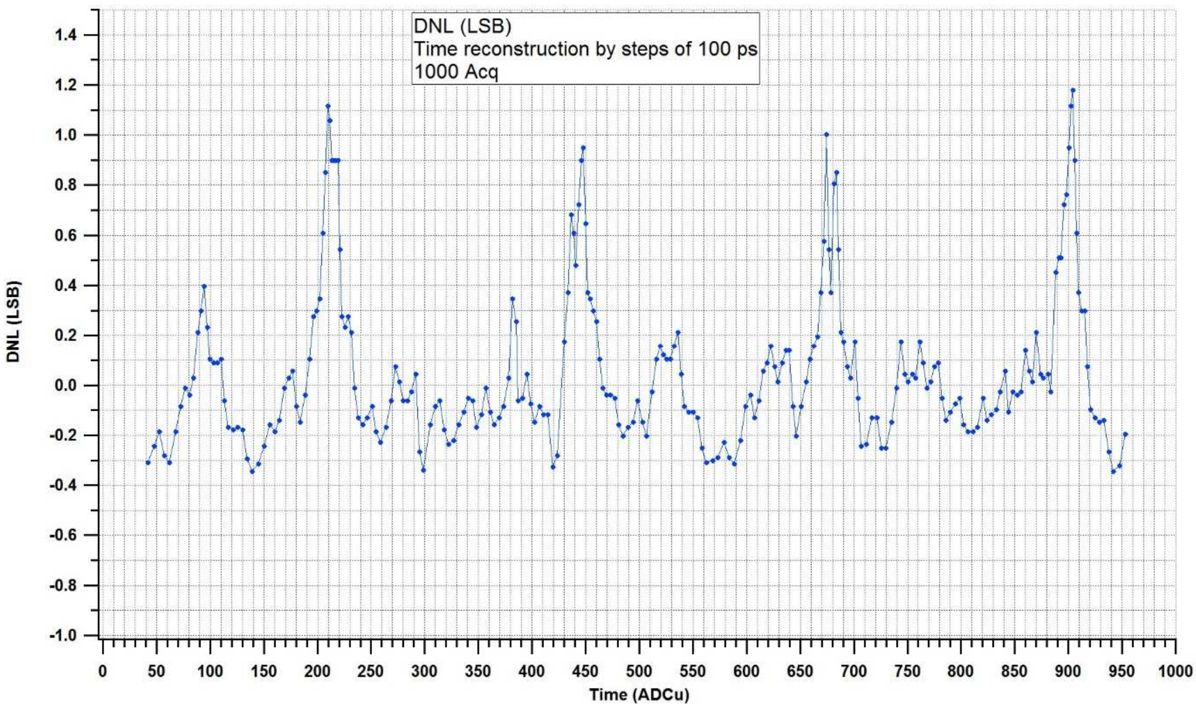

Figure 34 TAC DNL (# of LSB)

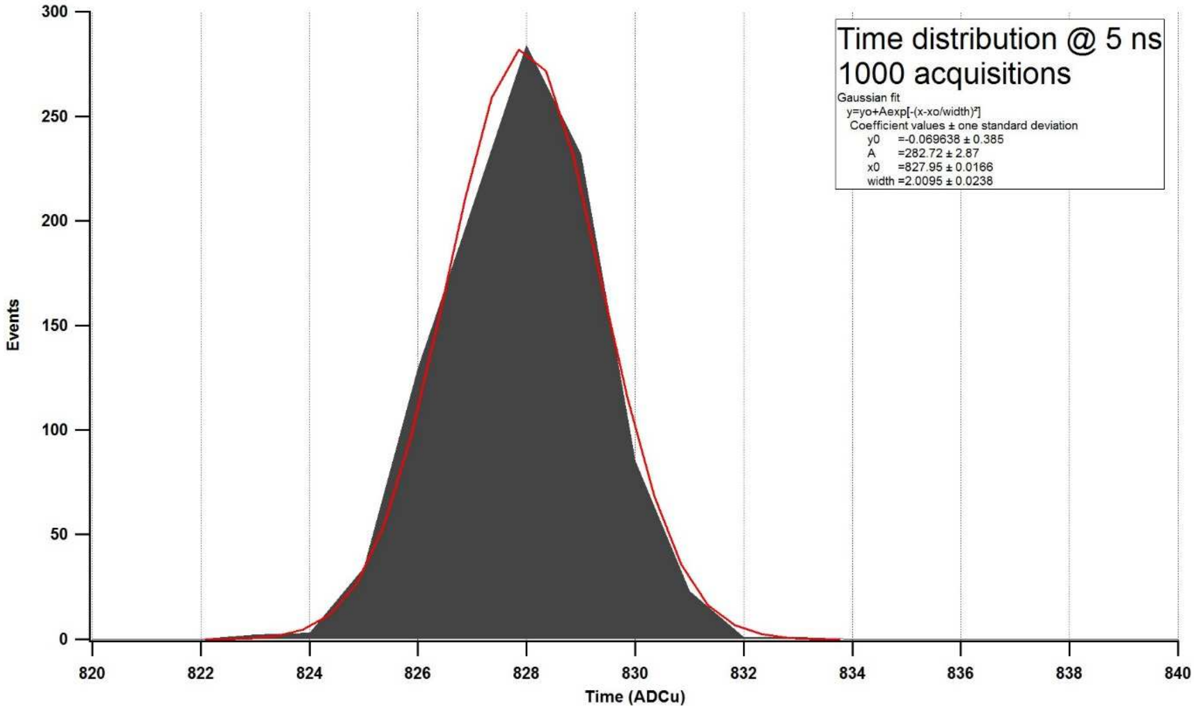

Figure 35 Time distribution with an input signal delayed of 5 ns. 1000 acquisitions.

The TAC ramp is implemented in each channel. The 16 ramps are reconstructed and are shown in figure 37. Fitting the ramps by a linear fit in figure 38, 39 and 40 are shown respectively the intercept (ADCu), the slope (ADCu/ns) and the LSB (ps/ADCu) of the 16 channels.

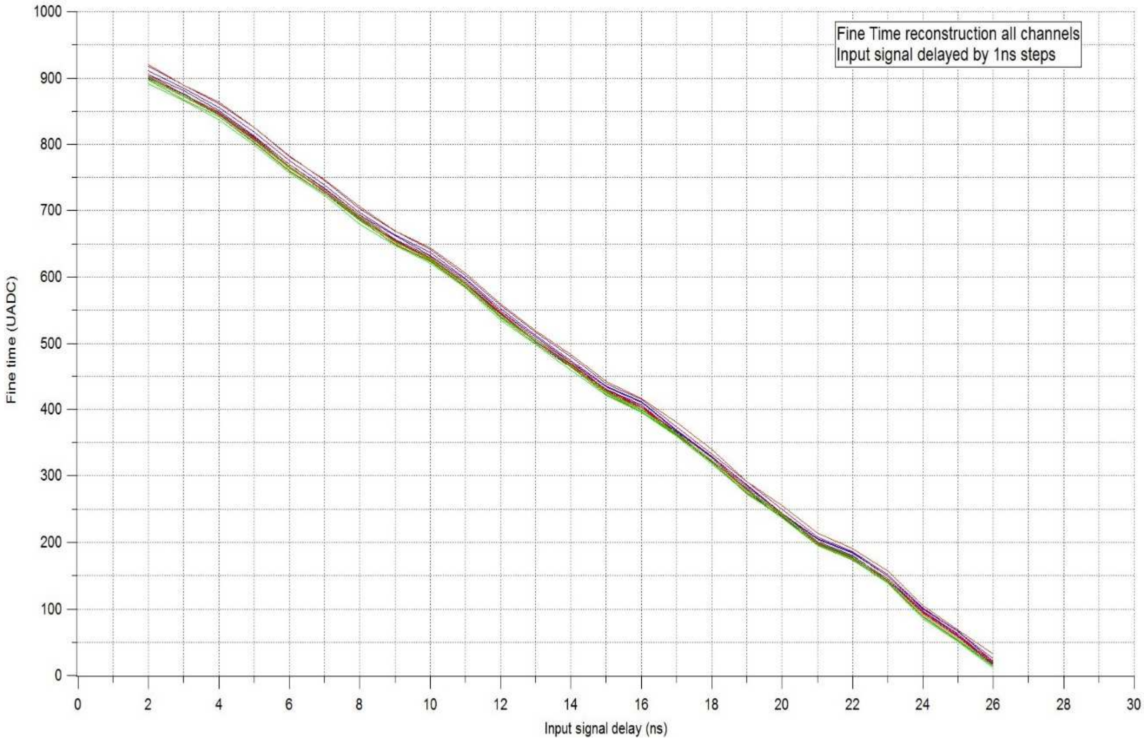

Figure 36 TAC ramps for the 16 channels

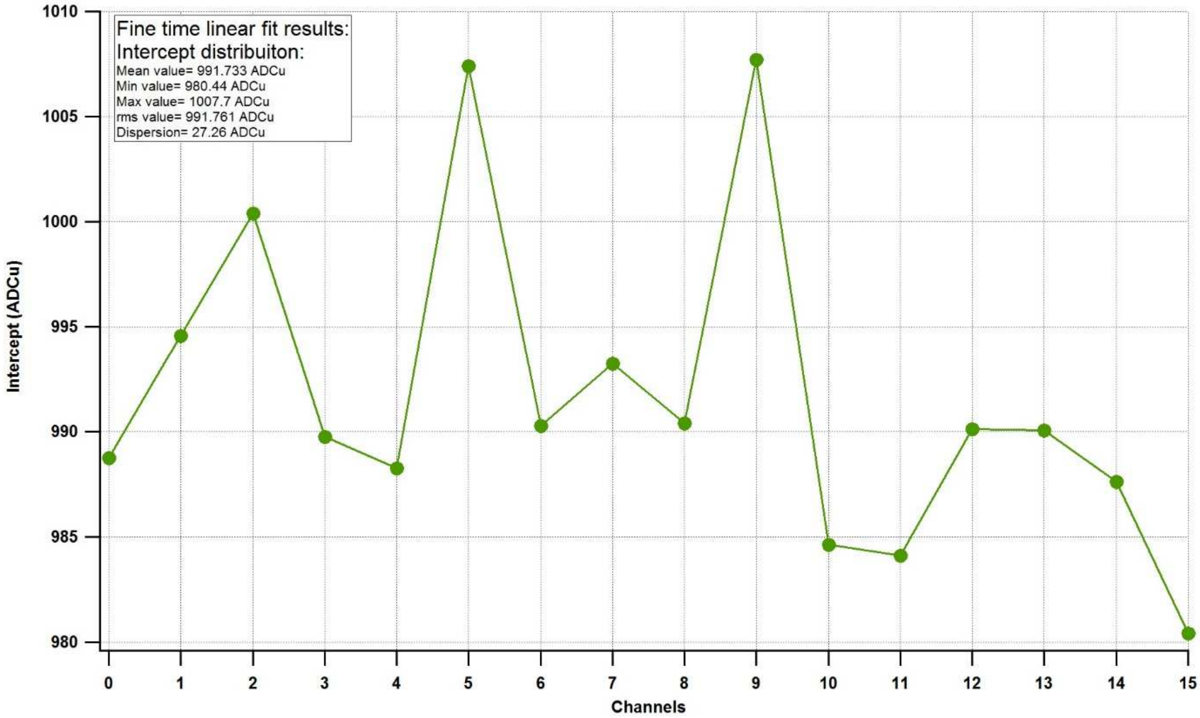

Figure 37 Intercept vs channels

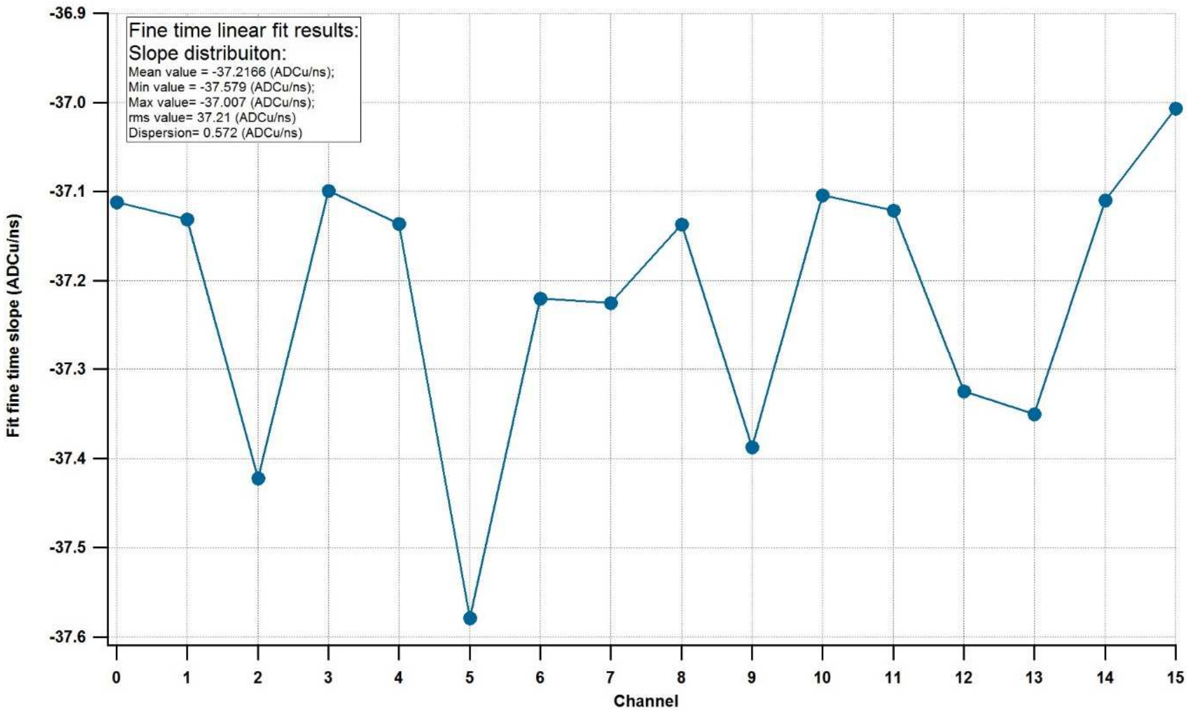

Figure 38 slope vs channels

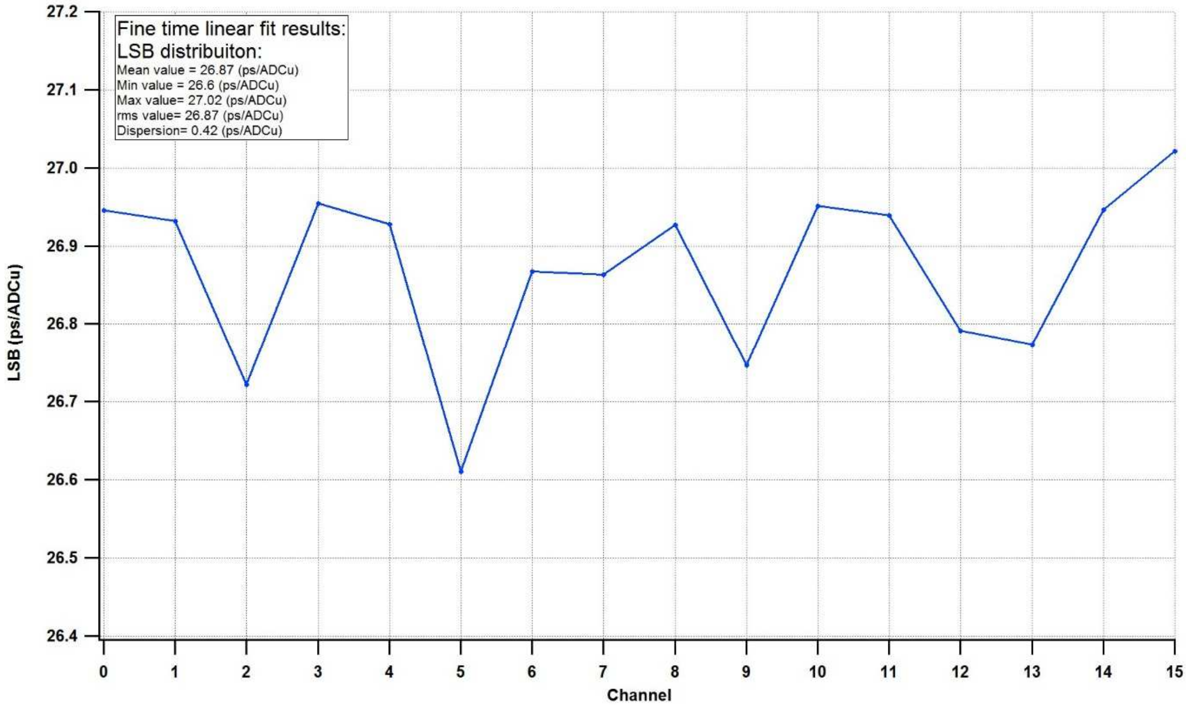

Figure 39 LSB vs channels

5 References