HGCROC: the front-end readout ASIC for the CMS High Granularity Calorimeter

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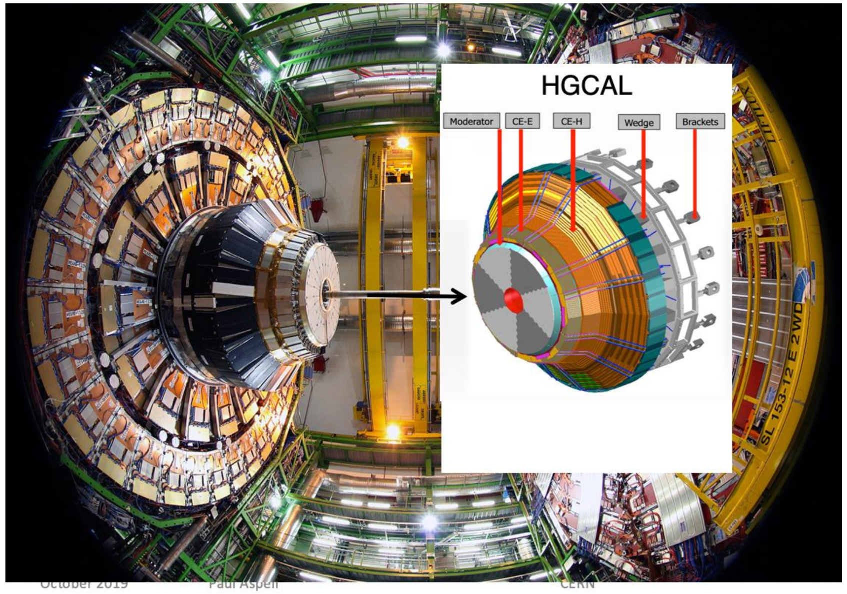
HGCAL: Endcap Calorimeters for the CMS Phase-II upgrade

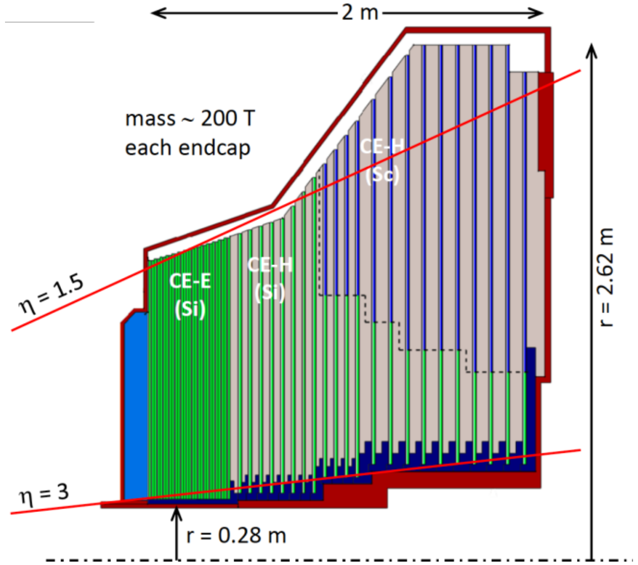
- **HGCAL covers 1.5 < eta < 3.0**

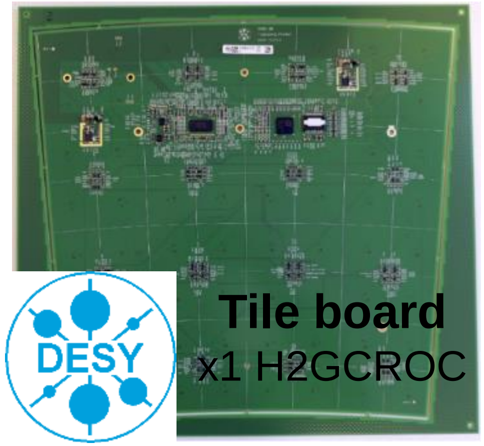
- Full system maintained at -30°C
  - ~ 640 m² of silicon sensors, 6.1M Silicon channels, 0.5 or 1.1 cm² cell size
  - ~ 370 m² of scintillators, 240k scintillator-tile channels

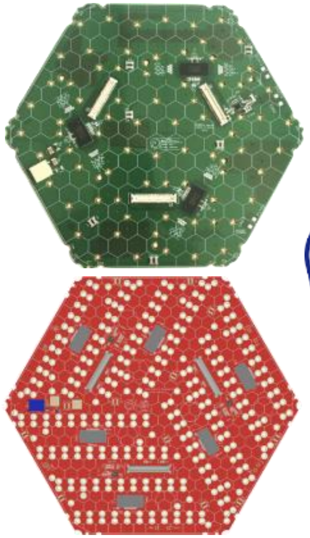
- Data readout from all layers
- Trigger readout from alternate layers in CE-E (Electromagnetic calorimeter) and all in CE-H (Hadronic calorimeter)

- Readout electronics: HGCROC
  - Two versions: Silicon and SiPM
  - Rad. tolerant (200 Mrad, 1.10^{16} neq / cm²)
  - Power consumption: 15 mW per channel
  - Noise: 0.4 fC
  - Charge: 0.2 fC to 10 pC
  - Pileup mitigation: Fast shaping (peak < 25 ns), precise timing capability (25 ps)



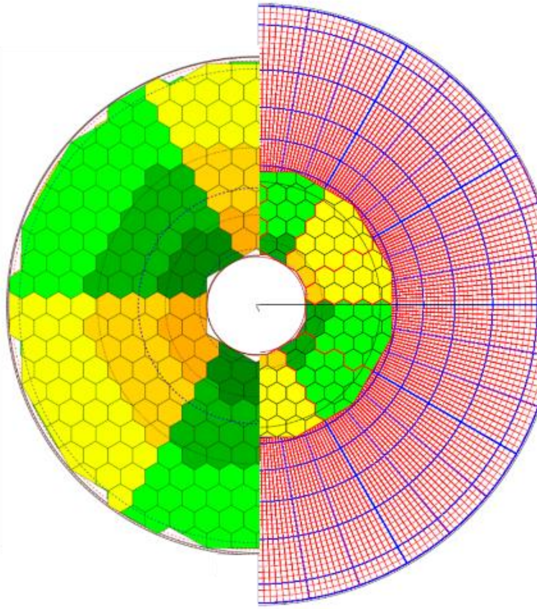






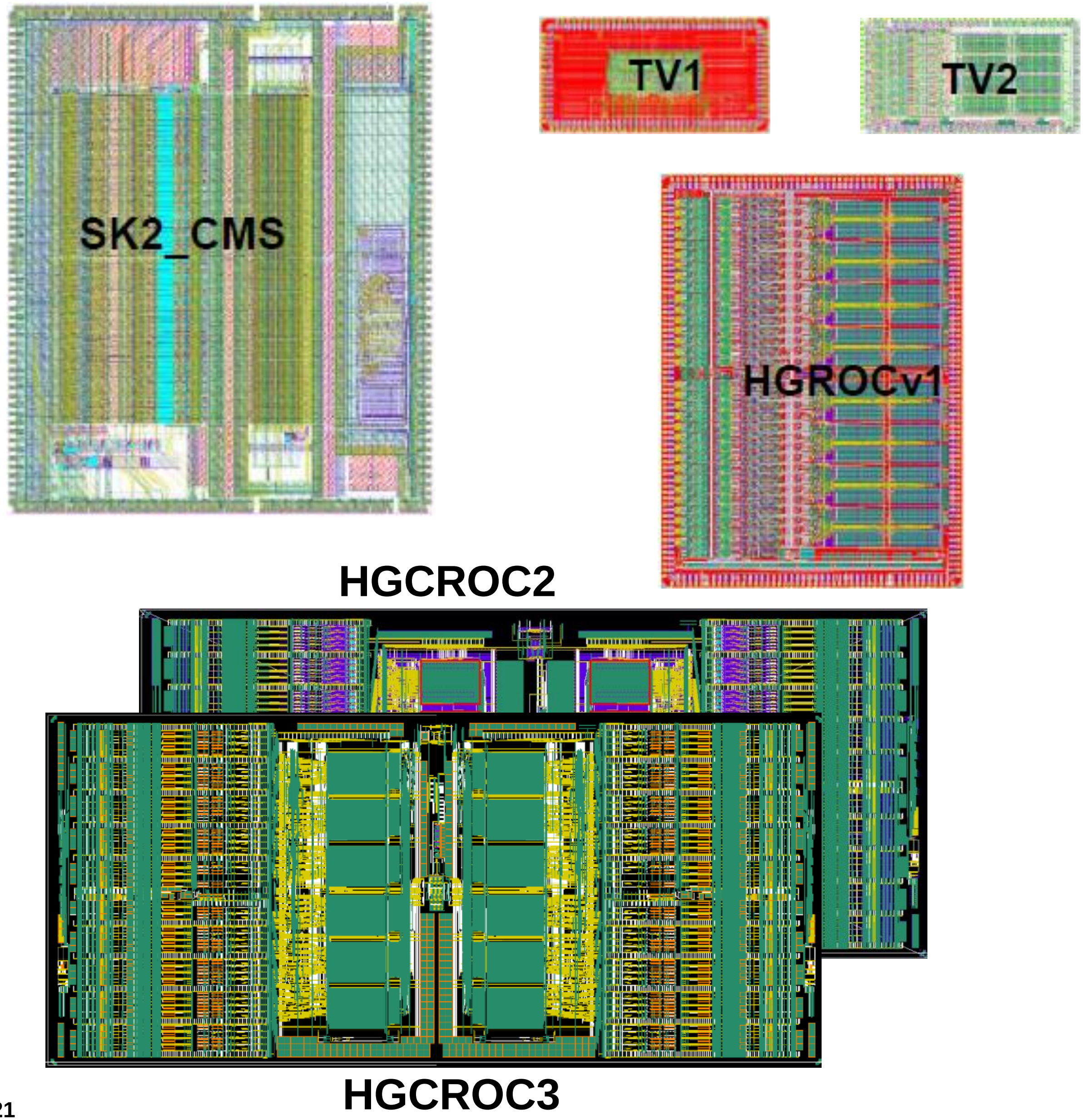
LD HB
x3 HGCROC

HD HB
x6 HGCROC



Development history

- Jan 16: SKIROC2_CMS [TWEPP 2016]
  - SiGe 350 nm 7x9 mm²
  - Dedicated to test beam and analog architecture (TOT)
- May 16: 1st test vehicle TV1
  - CMOS 130 nm 2x1 mm²
  - Dedicated to preamplifier studies
- Dec 16: 2nd test vehicle TV2 [TWEPP 2017]
  - CMOS 130 nm 4x2 mm²
  - Dedicated to technical proposal analog channel study
- July 17: HGCROCv1 [TWEPP 2018]
  - CMOS 130 nm 5x7 mm²
  - All analog and mixed blocks; large part of digital blocks
- Feb 19: HGCROCv2 [CHEF 2019]
  - CMOS 130 nm 15x6 mm²
  - Silicon and SiPM versions (for both 2 and 2A)
  - Final size, packaging and I/Os
  - 600 chips produced and packaged
- Dec 20: HGCROCv3 [This Talk] : Final Chip
  - Fully rad-hard digital Part
  - CMOS 130 nm 15x6 mm²
  - 1 additional memory stage
  - Back to the lab in July



HGCROC2 overview

Overall chip divided in two symmetrical parts

- Each half is made of:
  - 39 channels: 36 channels, 2 common-mode, 1 calibration
  - Bandgap, voltage reference close to the edge
  - Bias, ADC reference, Master TDC in the middle
  - Main digital block and 3 differential outputs (2x Trigger, 1x Data)

Measurements

- Charge
  - ADC (AGH): peak measurement, 10 bits @ 40 MHz, dynamic range defined by preamplifier gain
  - TDC (IRFU): TOT (Time over Threshold), 12 bits (LSB = 50ps)
  - ADC: 0.16 fC binning. TOT: 2.5 fC binning
- Time
  - TDC (IRFU): TOA (Time of Arrival), 10 bits (LSB = 25ps)

Two data flows

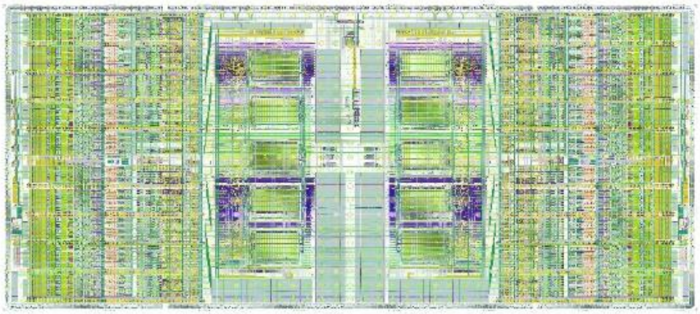
- DAQ path
  - 512 depth DRAM (CERN), circular buffer
  - Store the ADC, TOT and TOA data
  - 2 DAQ 1.28 Gbps links (CLPS)
- Trigger path
  - Sum of 4 (9) channels, linearization, compression over 7 bits
  - 4 Trigger 1.28 Gbps links (CLPS)

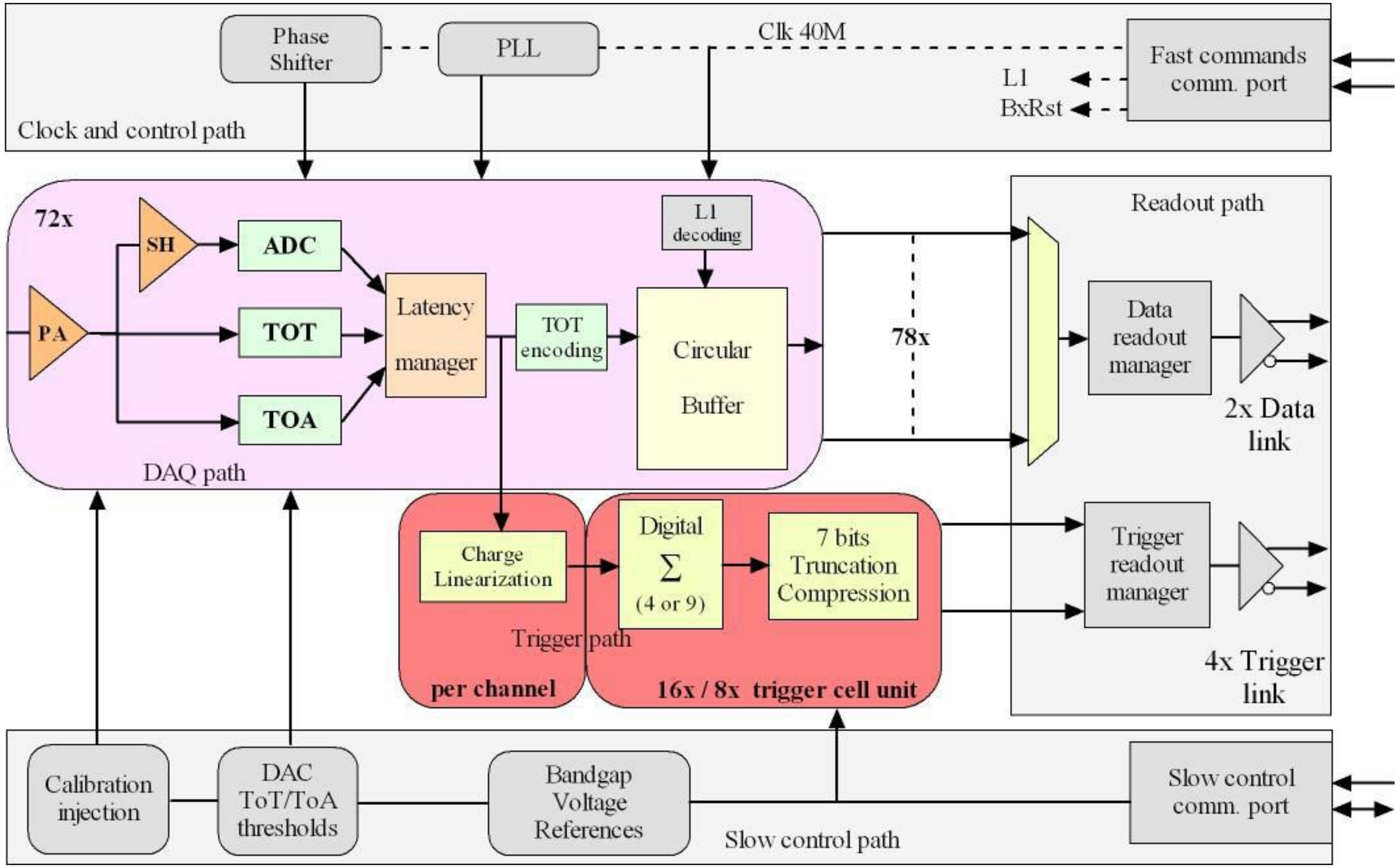
Control

- Fast commands
  - 320 MHz clock and 320 MHz commands
  - A 40 MHz extracted, 5 implemented fast commands
- I2C protocol for slow control

Ancillary blocks

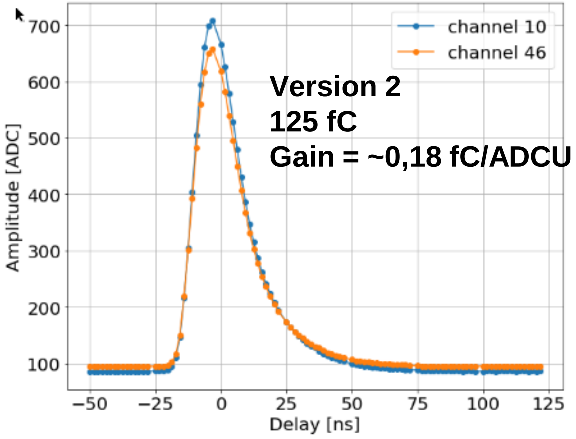
- Bandgap (CERN)
- 10-bits DAC for reference setting
- 11-bits Calibration DAC for characterization and calibration
- PLL (IRFU)
- Adjustable phase for mixed domain



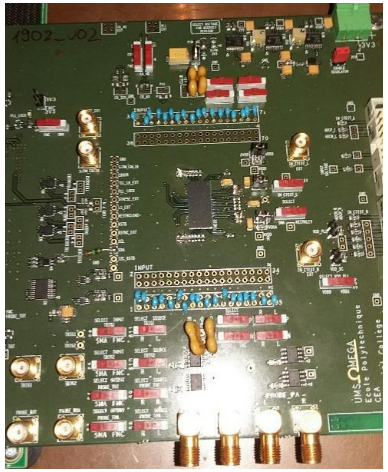


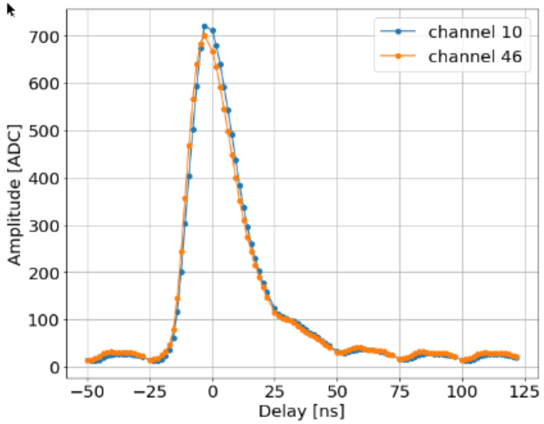
ROCv2 test boards - pulse scan reconstruction

Flip-Chip on mezzanine

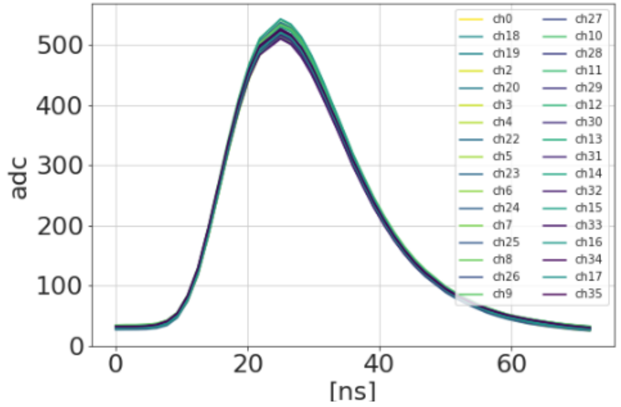


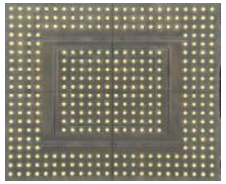
BGA board

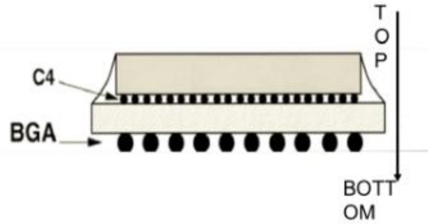




BGA on mezzanine



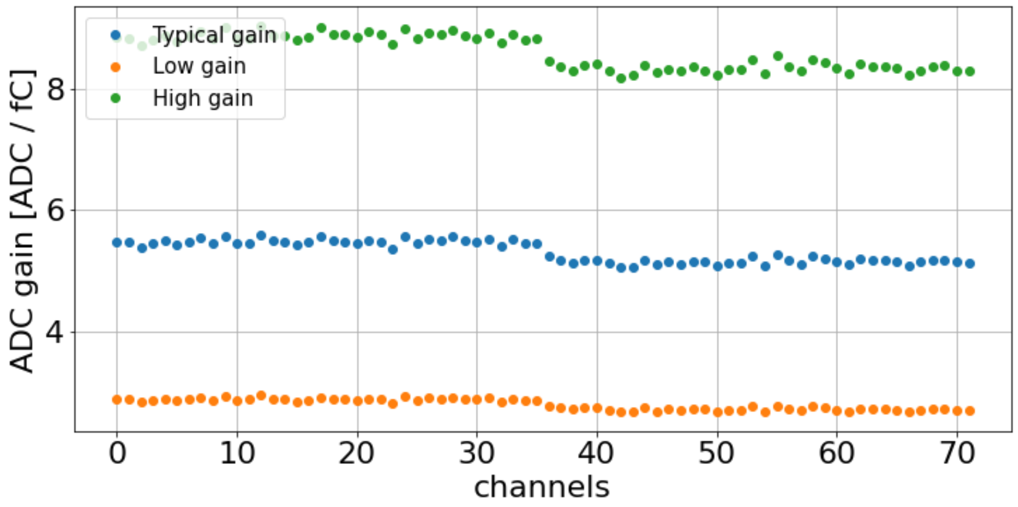


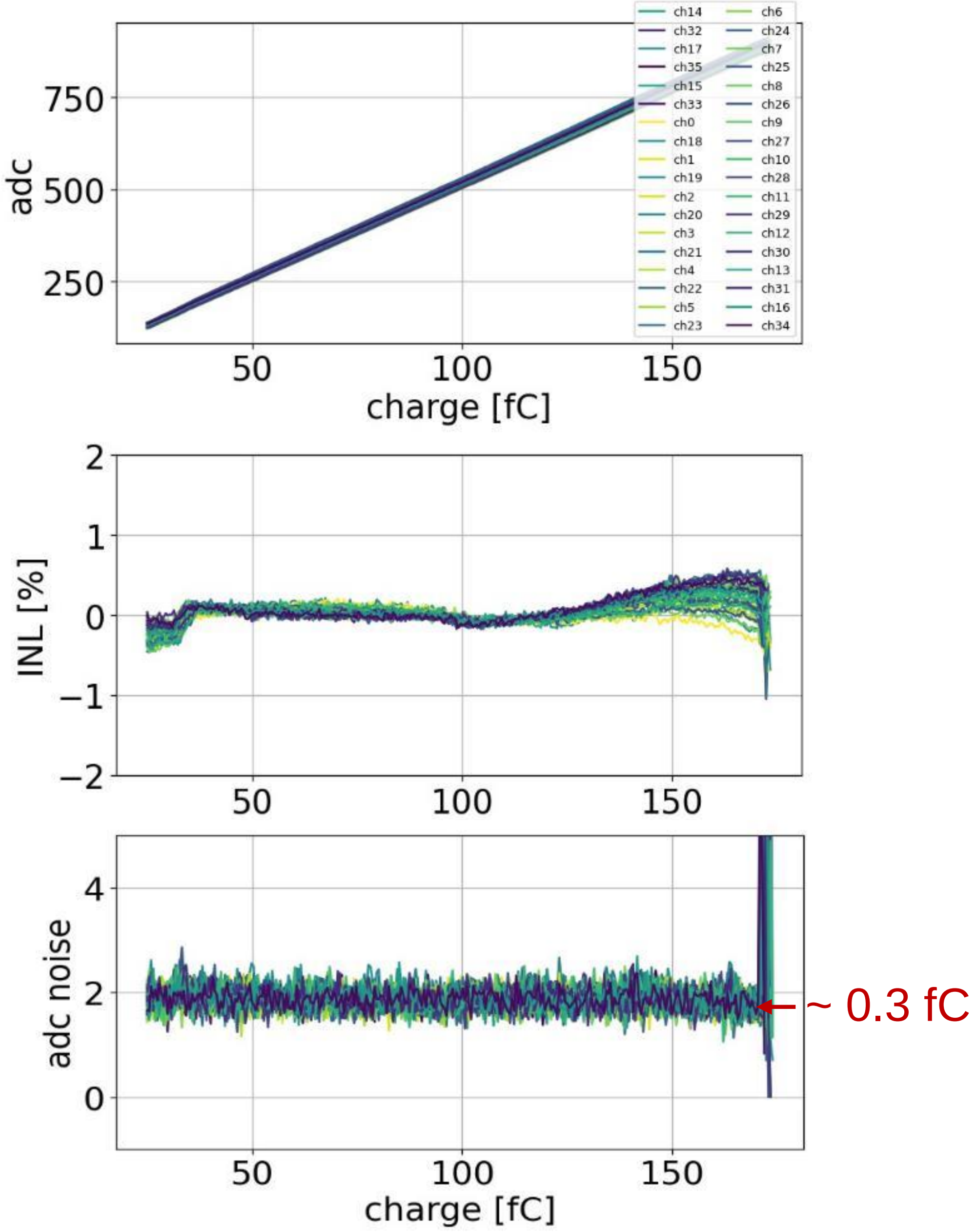


- Using phase shifter to move the sampling clock
- Separates effects from the BGA substrate and PCB
- Falling time (10-90 %): ~ 30 ns, < 20 % at BX+1
- Digital 40 MHz clock coupling on the analog signal on the BGA board (digital noise)

ROCv2: charge measurements: ADC range (0 – 160 fC)

- Two 10b-DAC to globally set the pedestal to a desired level
- 5b-DAC to reduce dispersion per channel
  - From ~ 100 ADCu dispersion to ~ 5 ADCu
- Good linearity within +/- 0.5%
- ~ 0.3 fC resolution with 50 pF input capacitor
- Good gain uniformity over the channels

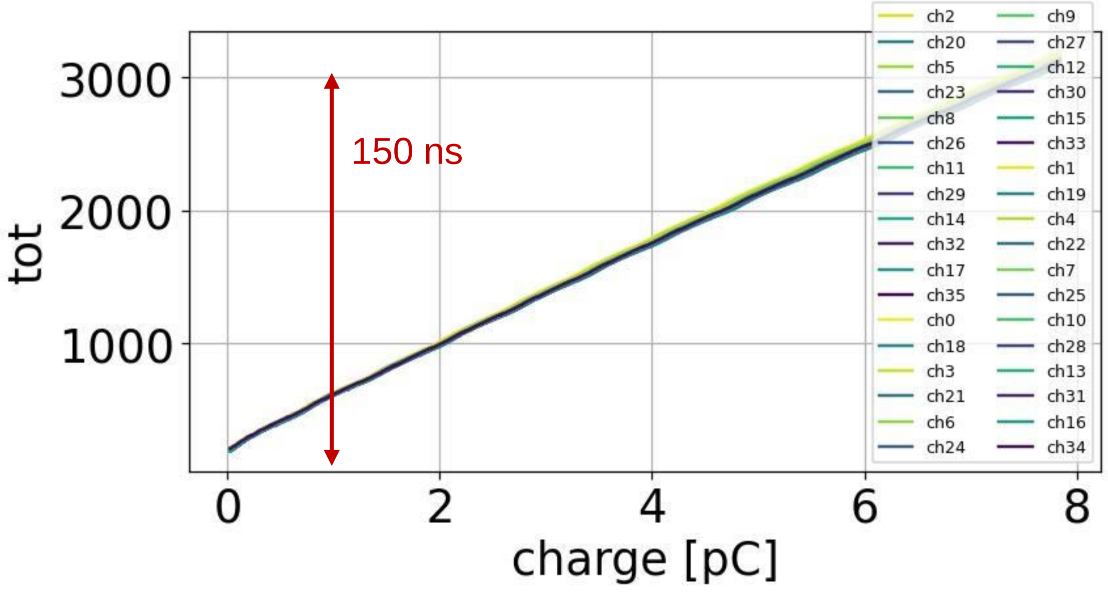


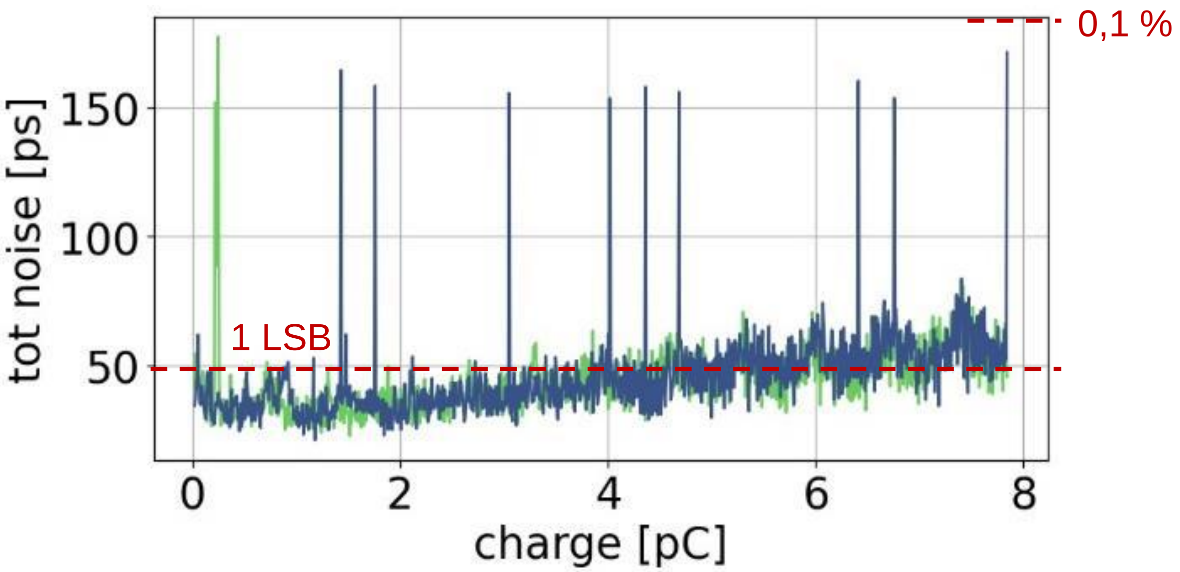


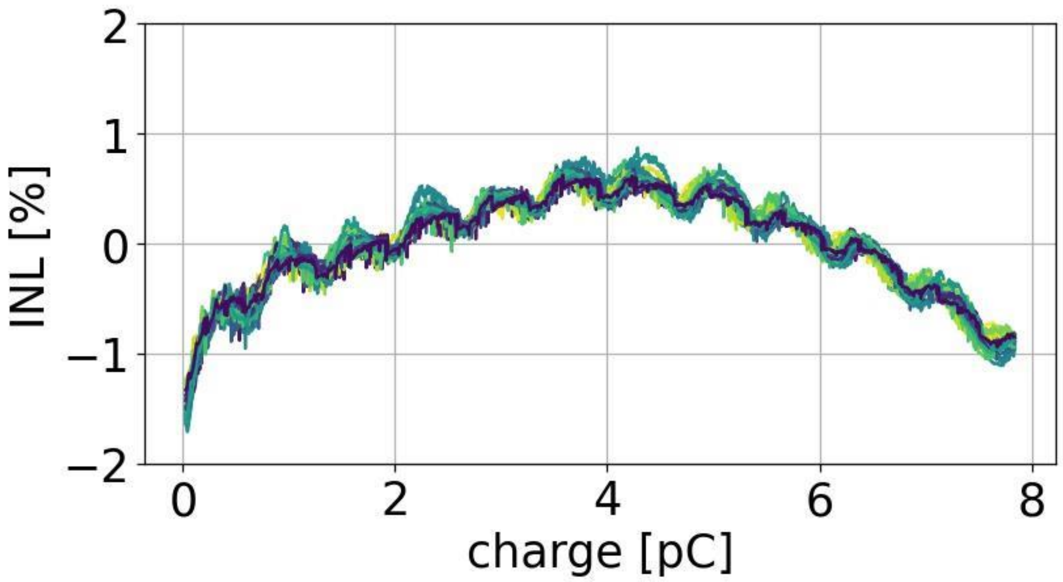
ROCv2: charge measurements: TOT range (160 fC – 10 pC)

Charge measurement from TOT when preamplifier saturates

- 160 fC to 10 pC (for the typical preamplifier gain)
  - 12 bits over 200 ns (LSB of 50 ps)
- Linearity < 2% linearity
  - Small residual wiggles on TOT (digital noise on preamplifier input)
- Resolution around the LSB (~ 50 ps)
  - Some peaks due to outliers (understood and fixed)

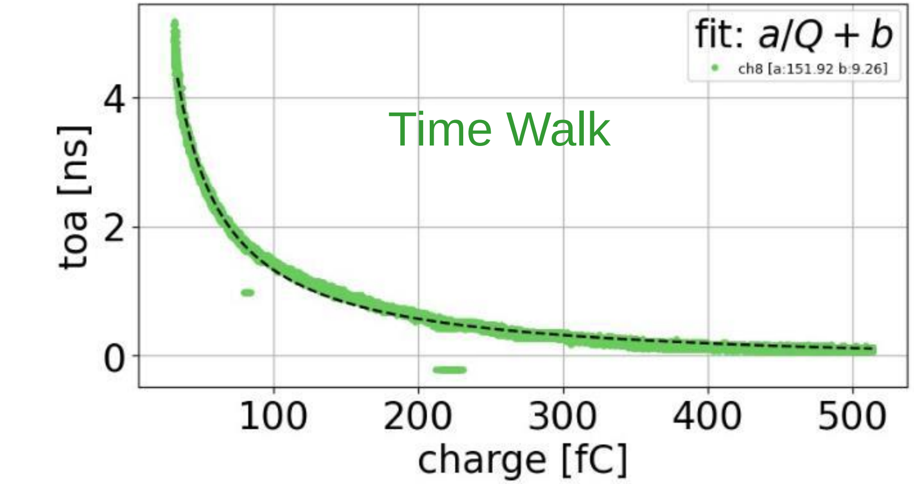


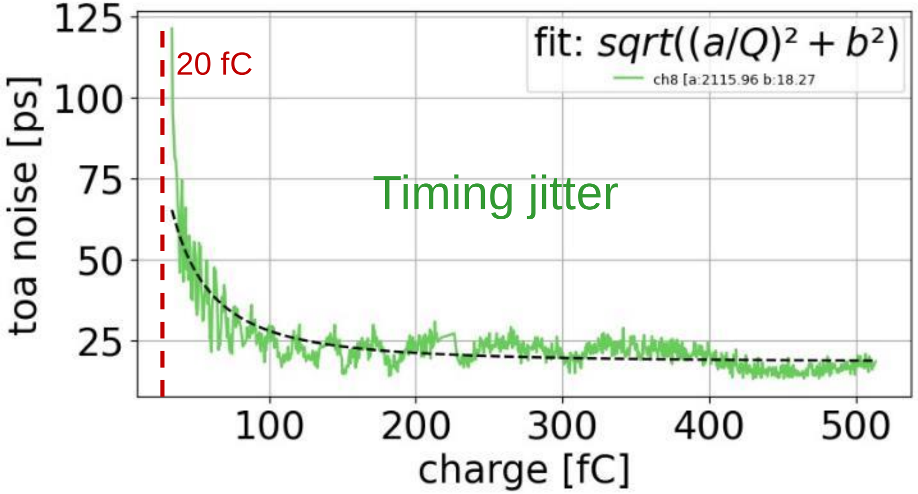


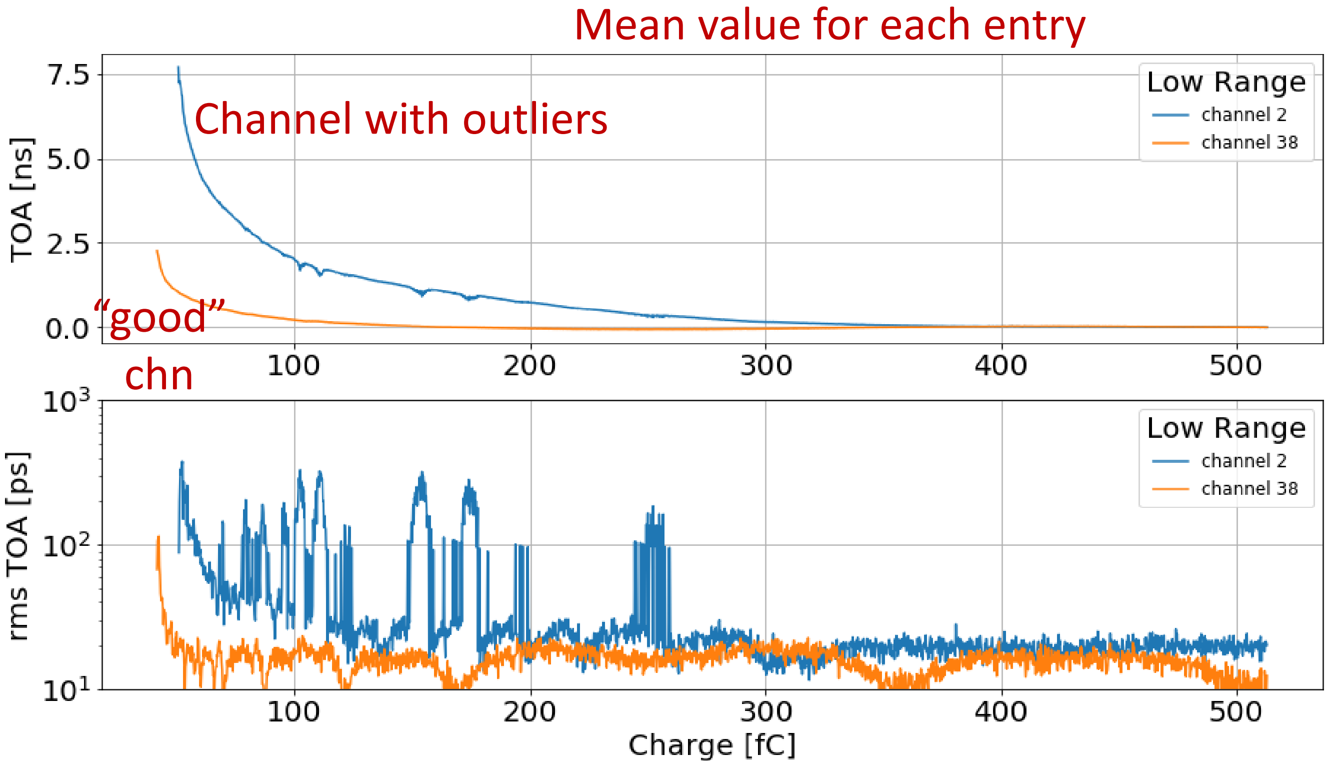


ROCv2: Timing performance (TOA)

- Minimum threshold for a TOA measurement is 20 fC (limited by the digital coupling)
- Some outliers seen in raw data (left plots)
- Plotting mean value highlights this in some channels (right plots)



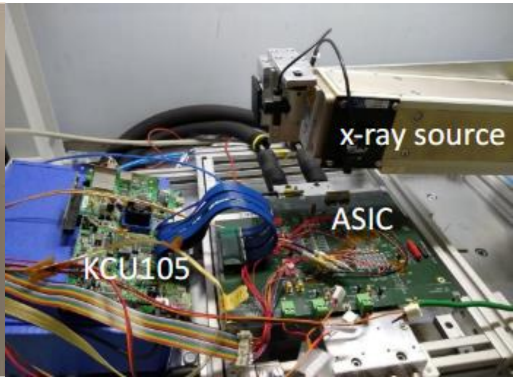


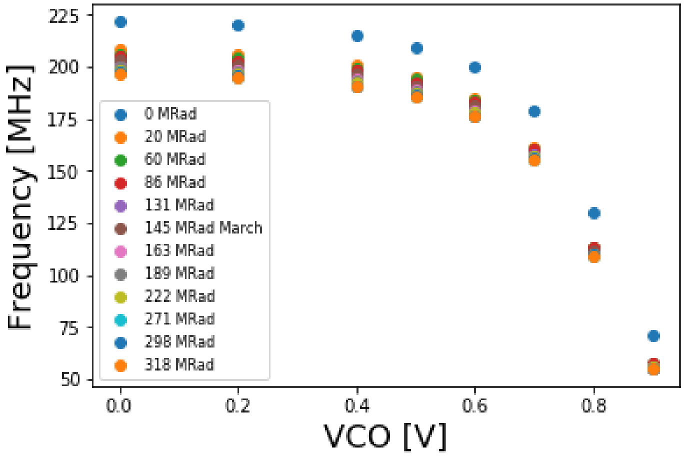


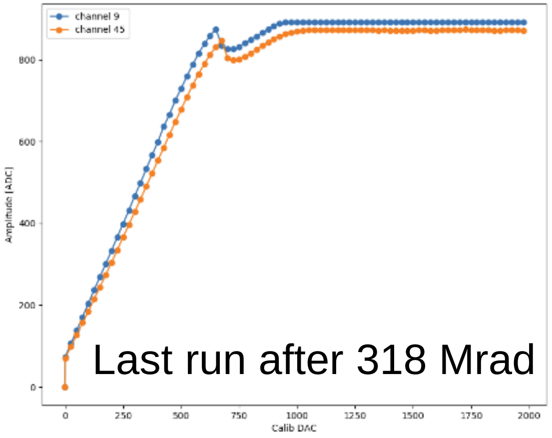
TID and SEU tests [P. Everaerts, L. Ceard]

TID: thinned chip (70 µm)

- 3 campaigns at CERN:
  - Si-version at room temperature (Oct 2019)
  - Si-version at cold (Mar & Jun 2020)
  - SiPM-version at room temperature (Aug 2020)
- Irradiation up to 310 Mrad (5 Mrad for SiPM)
- The chip still works after annealing

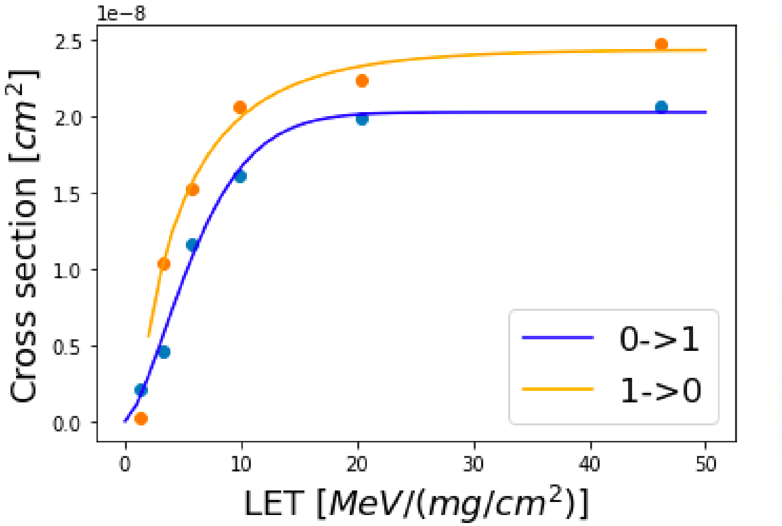




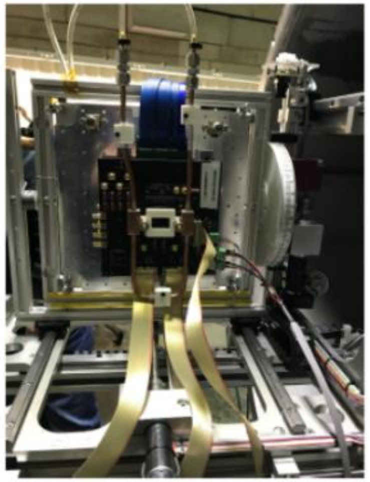


SEE: 2 campaigns at Louvain (Nov 2019 & Feb 2020)

- **Heavy ions LET 5 – 45 MeV**
- I2C acted as expected: cross section follows the usual curve and **no errors recorded when auto-correction set. Flips < 2 E-7 Hz/chip**
- Bit shifting in the DAQ link (no triplicated Serializer in HGCROCv2)
- No signs of latch-up effects
- No flips seen in ADC/TOA/TOT data



Inside the vacuum chamber



HGCROC3: final version

Analog Upgrades:
- Increased sensor leakage current compensation
- Increase resolution (12bit) of DAC and phase shifter for calibration
- TOA calibration with a Randomized Pulse Generator

Triplicated Logic
- Memory pointers and calculation logic

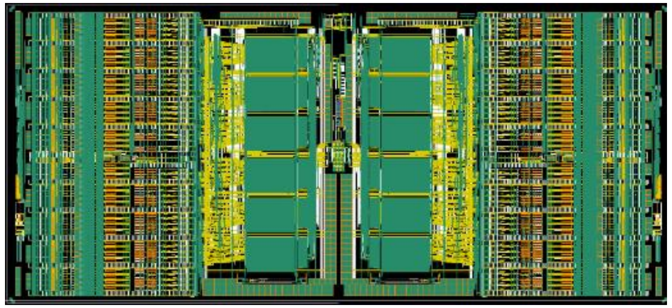
High Speed Serial links
- SEE tolerant

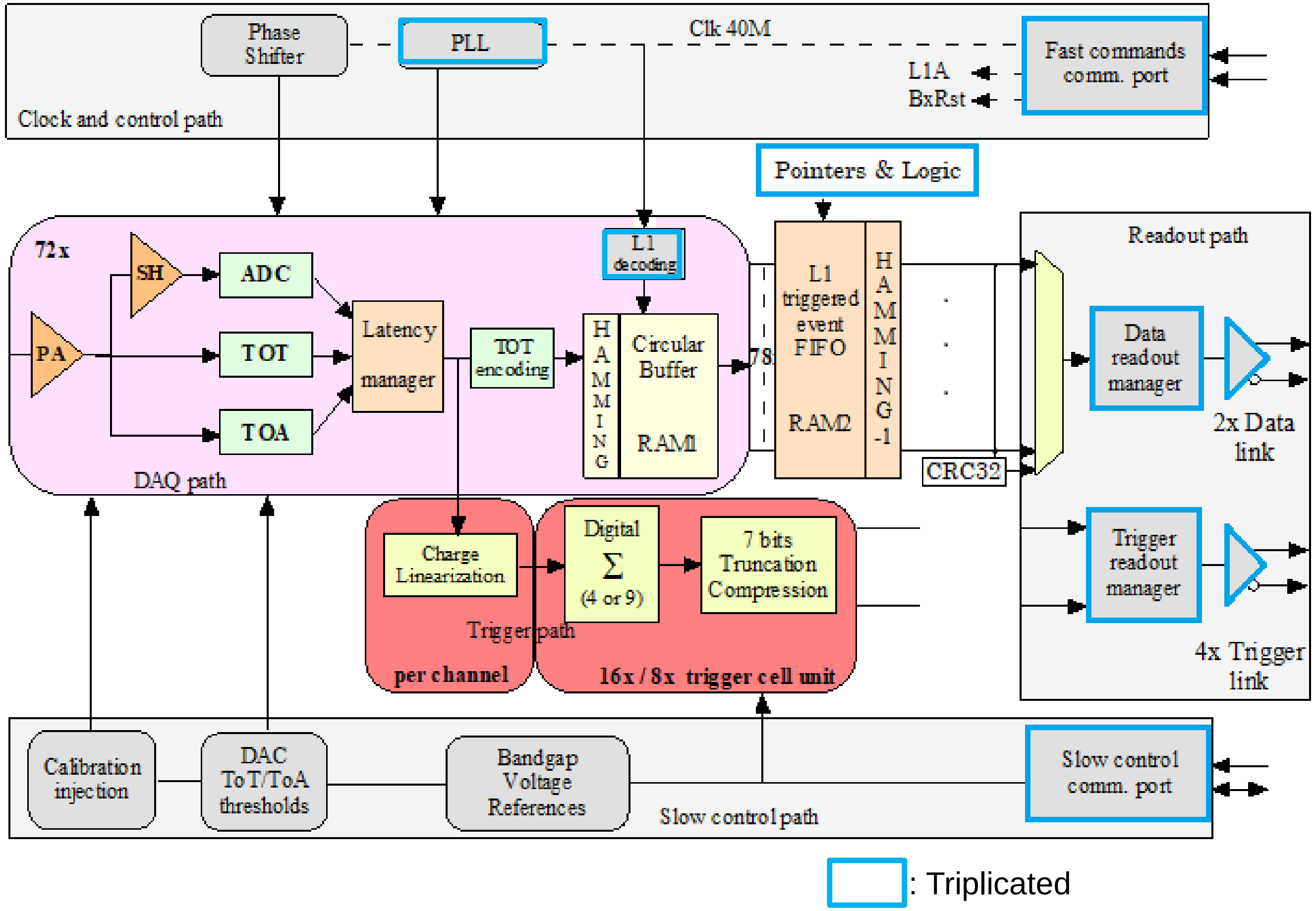
Control
- SEU tolerant Fast commands
- SEU tolerant I2C Module for slow control

Memory blocks
- Adds trigger derandomizing buffer for DAQ path
- Custom Hamming Encoding at the entry of Circular Buffer
- Hamming Decoding after the L1 FIFO

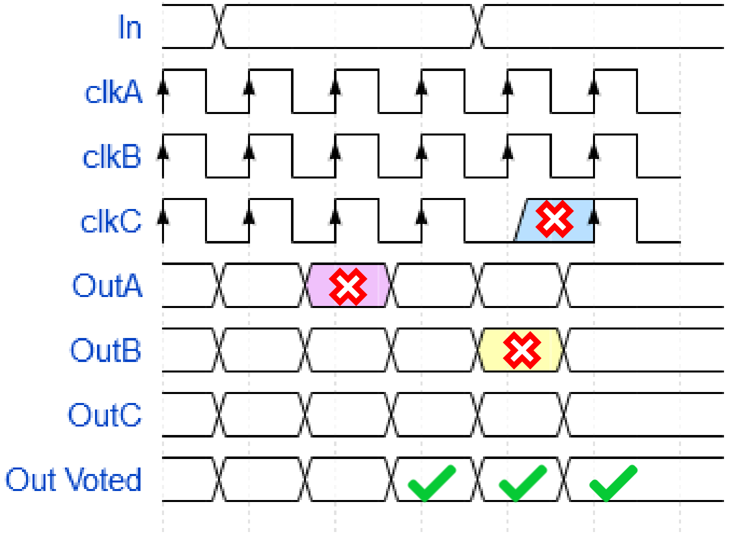
Checksum
- CRC-32 Checksum Encoding before serialization

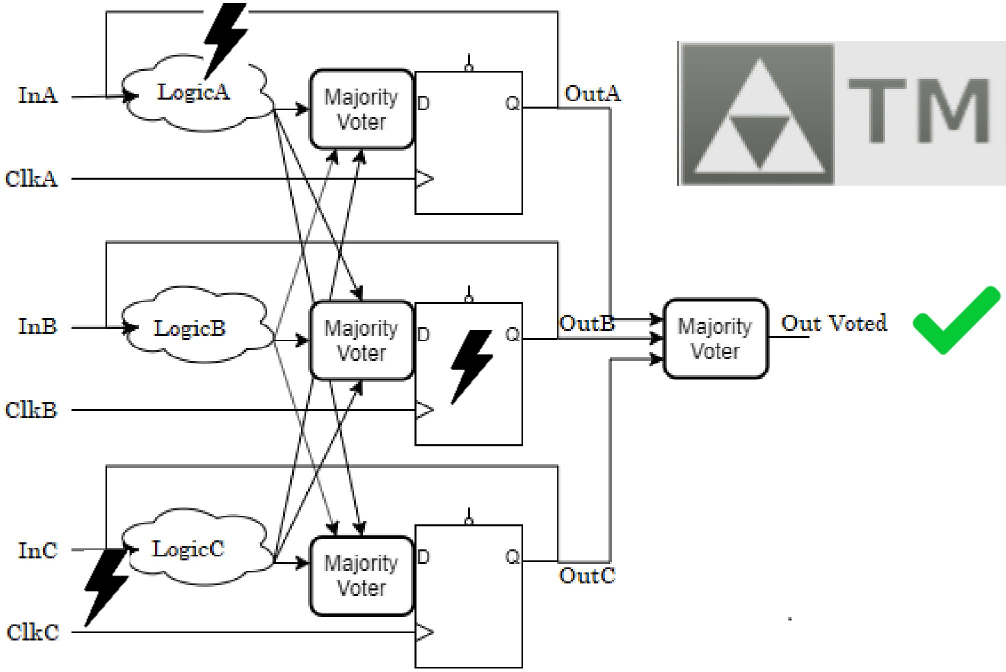
First measurements July-August 2021





- All the control logic was fully triplicated thanks to the TMRG tool:
  - 3 registers / 3 combinatorial logic
  - 3 majority voters (one in each path)
  - Majority voter on the output





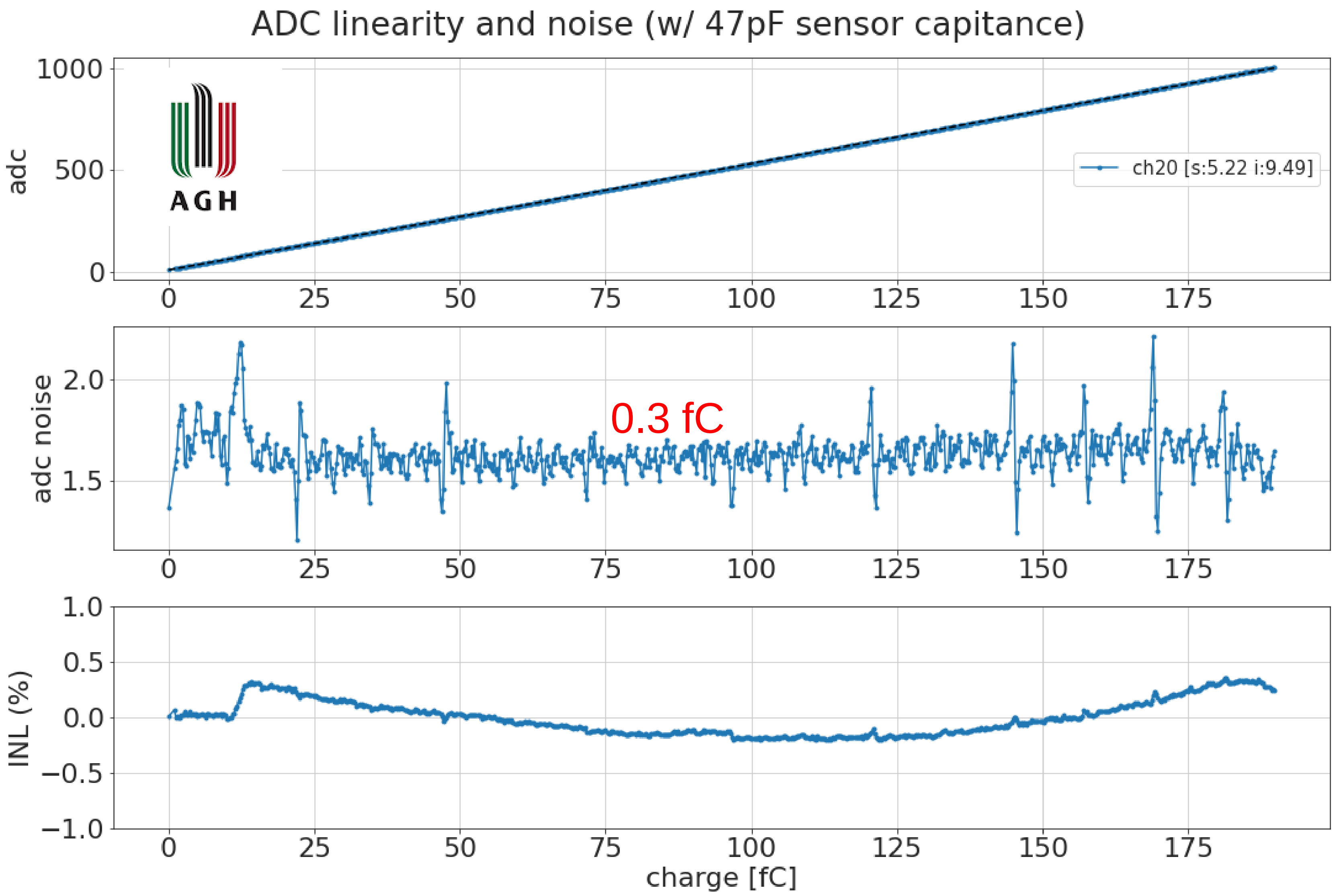
- Applied to 20% of the registers in the ASIC ➔ power consumption doubled (simulation from HGCROC2 to v3)
- Triplication applied to critical modules: state machines, pointers, counters and parameters
- Datapath protected in memories with SECDED code (Hamming)

ROCv3: Charge measurements (ADC range)

- Injection and readout with the full readout chain enabled
- Internal injection with calibration DAC (low 1,5 fC offset)
- ADC noise ~0.3 fC resolution (1.6 ADCu)
- Good linearity within +/- 0.5%

➔ The results are comparable to ROCv2 in terms of noise and linearity

Preliminary results

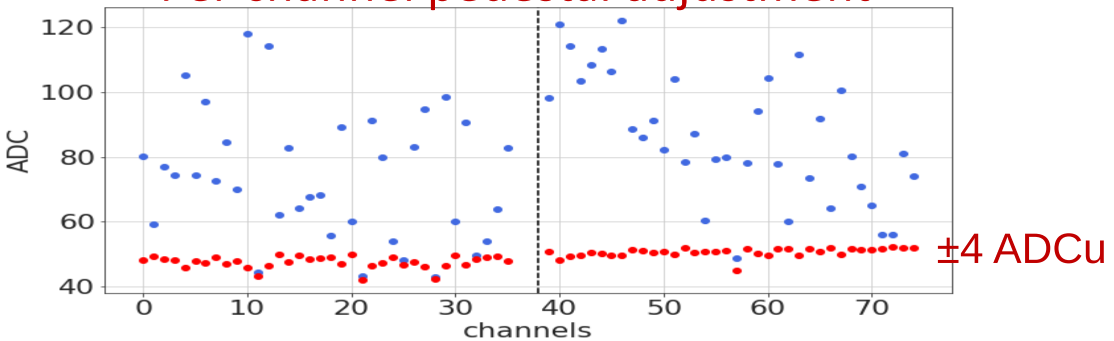


ROCv3: Noise and pedestal measurements

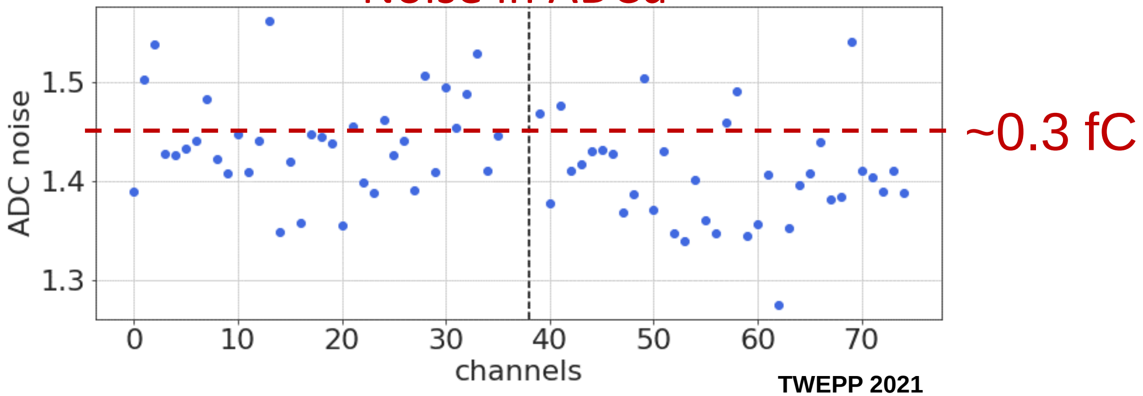
- Measured noise with 50 pF input cap = 0.3 fC (~ 2000 electrons) (0.7 nV / √Hz)
- Very low correlated noise contribution: max 0.15
- Comparable with HGCROC2 even if the digital activity was doubled

- ADC pedestal adjustment done manually with local 6b DAC

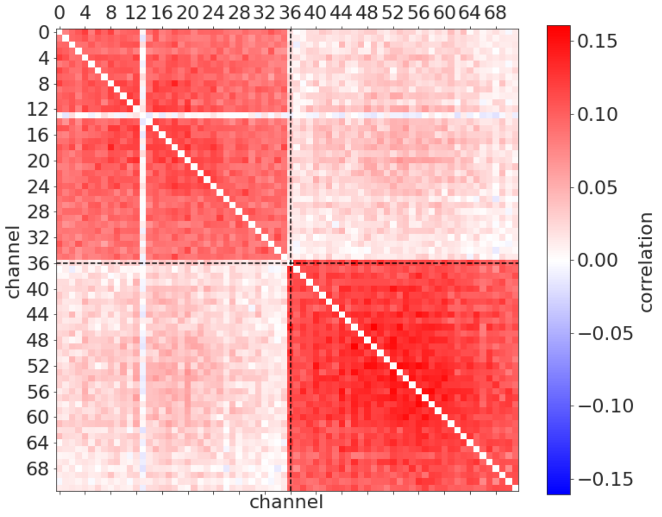
Per channel pedestal adjustment



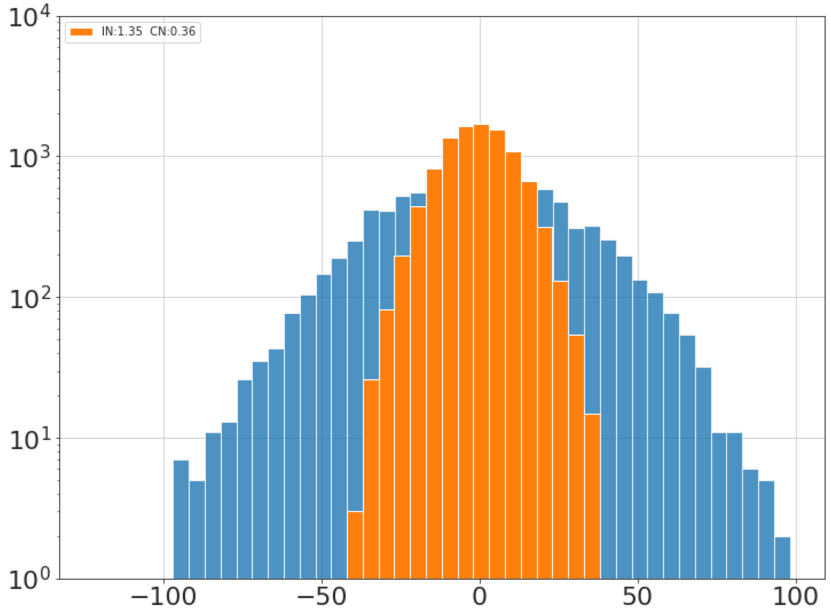
Noise in ADCu



Correlation [chip 0]

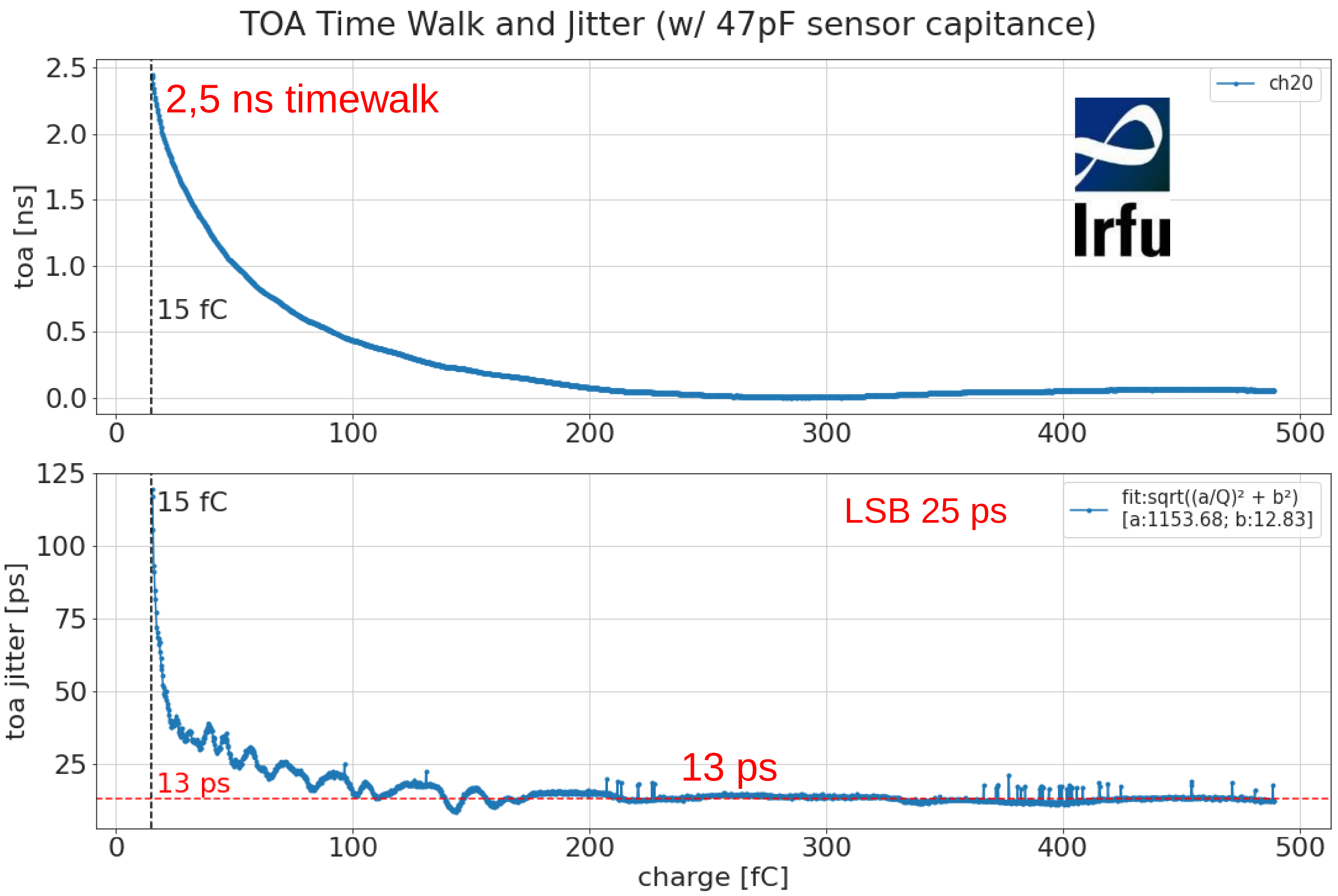


Full chip (72 channels)



ROCv3: Timing measurements (TOA)

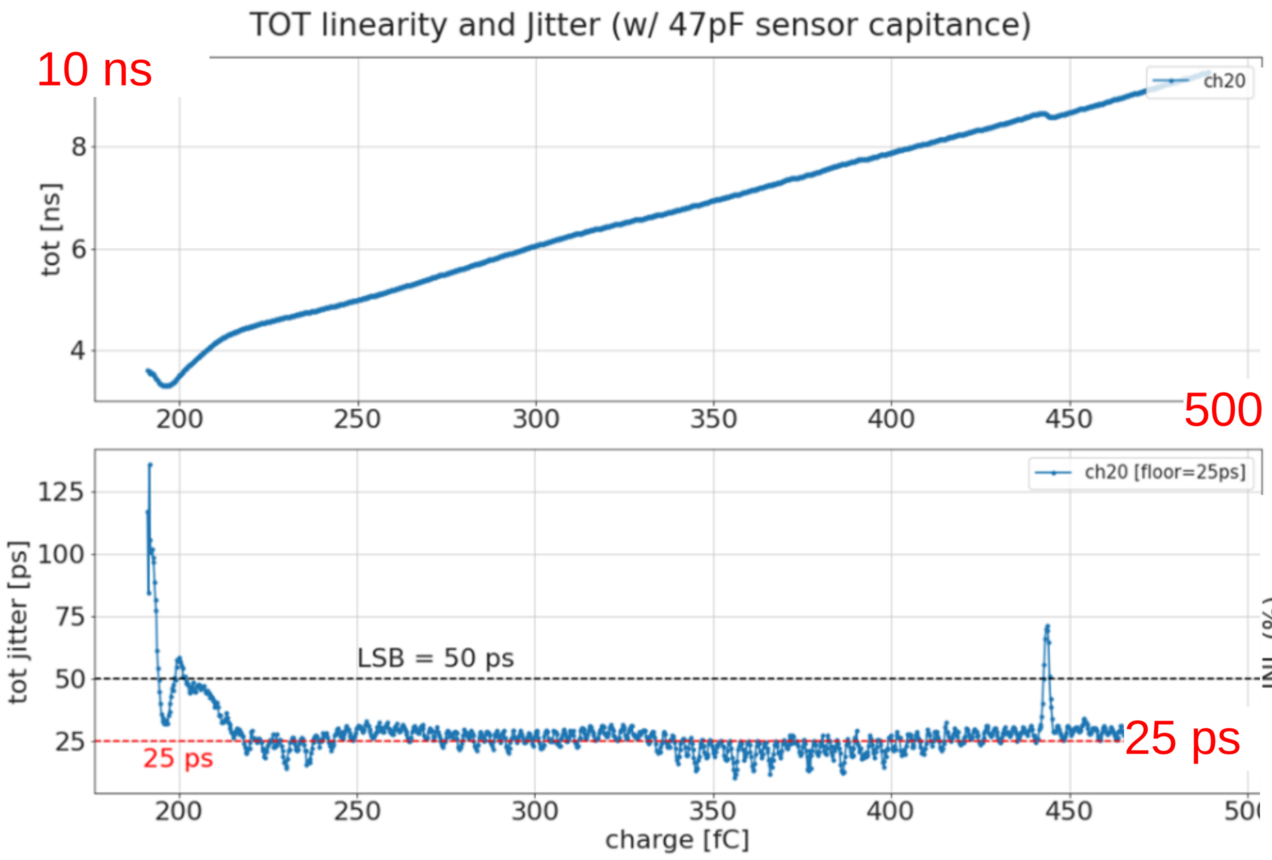
- The TDC has been improved to properly reconstruct the timing (also new layout) and to cope with outliers
- Minimum threshold set to 15 fC (20 fC for ROCv2)
- The measured jitter is about 13 ps (25 ps for ROCv2)
- Extremely promising results

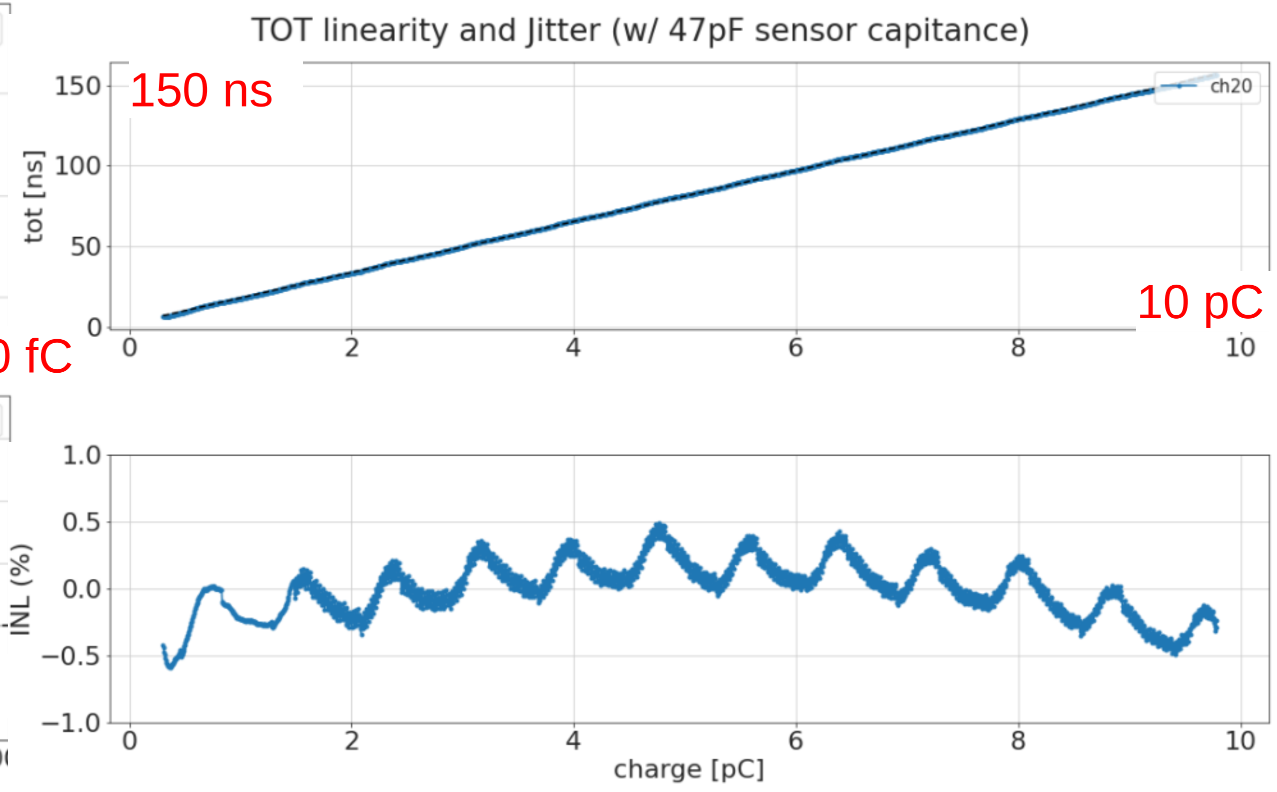


ROCv3: Time over Threshold measuremenst (TOT)

Charge measurement from TOT when preamplifier saturates (max 200 ns)

- 160 fC to 10 pC (for the typical preamplifier gain) with 12-bits TDC (LSB 50ps)
- Linearity < 1% linearity to be confirmed (2% in ROCv2)
- Resolution around 25 ps (50 ps in ROCv2)





Summary

- With HGCROC2, a big step was taken to reach HGCAL requirements. It is an extremely complex chips designed for imaging calorimetry: high dynamic charge, precision timing measurements, high speed links, a lot of digital, harsh radiation environment…

- Measurements are well understood for both Silicon and SiPM versions @CERN, LLR, IRFU, Desy and OMEGA
  - Charge performance reaches the specification: 1 % linearity, for both ADC and TOT
  - Timing performance: time walk calibration feasible, jitter below 25 ps
  - SEEs appear only in the non-triplicated parts of the chip (as expected)

- HGCROC3 integrates all the functionalities + a fully radiation tolerant digital part.
- The first measurements are encouraging but we are only at the beginning:
  - Charge linearity within 1%
  - TOA and TOT jitter less than 13 ps and 25 ps respectively

- Need to check the SEE robustness and to perform systematic measurements to confirm the results

- LLR and OMEGA designing and setting up 2 robots to perform ASIC production testing (foreseen end of 2022)