



Organization for Micro-Electronics design and Applications

High Granularity Timing Detector in HL-LHC



Talk on the long Flexible Printed Circuits



Flex PCB

Sensor

ALTIROC

Wire bonding

SIC'S REQUIREMENTS	from Marisol Robles Manzano on Thursday, 9h20
5 channels nimum charge : 2 fC harge dynamic : up to 100 fC ise : < 0.5 fC or 3 ke ⁻	TOA TDCResolution: 20 psMeasurement window: 2.5 nsConversion time: < 25 ns
oss-talk: < 2 %	TOT TDCResolution: 120 psDynamic range: 20 ns
libration LGAD-like injection :	Conversion time : < 25 ns
se time : 0.5-1.5 ns	Radiation tolerance
minosity : Number of hits per nch crossing for 2 time windows	NIEL : 2.5 $10^{15} n_{eq}/cm^2$ w/SF=1.5 SEE : $10^{15} n_{eq}/cm^2$ w/SF=1.5 SEU rate : < 5 % per hour
onding /	ASIC power dissipation < 1.2 W
Connector Assembling with insulating glue Bump bonding	Per channel : Analog very front-end : < 2 mW TDC : 0,5 mW at 10 % occupancy Digital : < 2 mW

ALTIROC's architecture



Analog front-end pixel

PLL

phase shifter

calibration pulser



Digital part of the pixel

End Of Column Luminosity process unit 320 Mbit/s fast commands decoder Trigger Processing unit Hit data transmission up to 1,28 Gbps Slow Control

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Pixel analog front-end





ALTIROC2's pixel integrates :

- A voltage (VPA) or trans-impedance (TZ) 1 GHz preamplifier followed by a high-speed discriminator:
 - Time walk correction made with a Time over Threshold (TOT) architecture
 - Main challenge = small jitter (low noise/capacitance) down to 4 fC
 - \Rightarrow Analog FE performance crucial

$$\sigma_{jitter} = \frac{N}{dV/dt} = \frac{e_n C_d}{Q_{in}} \sqrt{t_d} \qquad \begin{array}{c} t_d: LG \\ Q_{in}: N \\ e_n: nG \end{array}$$

- C_d : sensor cap (~4 pF) t_d : LGAD drift time, 600 ps Q_{in} : MIP charge (10 fC at start, 4 fC at end) e_n : noise spectral density of input trans.
- **Two TDC** (Time to Digital Converter) to provide Time of Arrival (TOA) + Time Over Threshold (TOT) measurement
 - TOA TDC: bin of 20 ps (7 bits), range of 2.5 ns, to be centered on the bunch crossing
 - TOT TDC: bin of 120 ps (8 bits), range of 20 ns

Pixel digital back-end



Hit buffer: SRAM 1536 x 19 bit •

- Circular buffer to store timing data for each bunch-crossing, until a L1 trigger arrives
- Data = TOT and TOA bits, only in case of hit to save power; with zero suppress.
- Depth of about 38 µs

Trigger Hit Selector: ٠

- Each received trigger associated to a trigger tag
- If data stored in Hit buffer related to received trigger, TOA/TOT data + trig tag stored into Matched Hit Buffer

Matched Hit Buffer: 32 positions FIFO ٠

- Control Unit: looks for data related to a trigger event when requested by the End Of Column
- Matched flag handled through a priority OR chain. Pixel at the top of the column with highest priority
- Synchronous readout at 40 MHz

Testbench for ALTIROC2



- Setup = ASIC board (ASIC alone or bump bonded onto sensor) + interface board + FPGA board
- Front-end calibration : charge injection (0 up to 50 fC) using ASIC internal calibration pulser, controlled by the FPGA, synchronous to 40 MHz clock, ASIC alone: Cd=3,5 pF can be set by SC to mimic sensor capacitor
- TOA/TOT TDC calibration : ASIC periphery generates a trigger with tunable width and delay thanks to the phase shifted 640 MHz clock from the PLL + Random Phase Generator for DNL





What is the minimum detectable charge ? (Median at 50%)



Sensor effect on noise





Digital noise injected on the preamplifier ground gets amplified only when the impedance between the detector capacitance and the non-inverting preamplifier input is not zero : when the sensor is connected !

Fighting against digital activity

Omega



ASIC+HPK LGAD biased at -80V (B16) All TZ ON

mega



- Time-walk = convolution of the preamplifier rise time (300 ps) with LGAD rise time (600 ps)
- Skew between bottom and top of the column pixel : due to clock tree distribution

• Offline time-walk correction using TOT

Comparing measured time-of-arrival jitter with simulation



Is the internal detector capacitance equivalent to an LGAD's ?



Pulse reconstruction of a voltage preamplifier, between ASIC alone and ASIC + sensor :

Showing same amplitude & falling edge decay time \rightarrow the internal LGAD-like capacitance corresponds to 3.5 pF. Showing slightly slowly rising time \rightarrow partially explains worst jitter with sensor.

nega

Jitter depends on the charge, but also on the discriminator thres.



Threshold trade-off to maximise pulse slope (dV/dt), thus minimize jitter.

mega

mega

Jitter stability under TID irradiation

ASIC alone (B7) Pixels ON : Col 7 (VPA) or 8 (TZ)





TID : 220 Mrad Dose rate : 3 Mrad/h Temperature : 22°C

All DC values and TDC bin remain constant along irradiation.

Conclusions

ALTIROC2 : first 225 channels full matrix LGAD readout chip with 1 GHz preamplifier with 4 pF detector capacitance : new territory in HEP !

- Analog performance demonstrated with ALTIROC2 are encouraging !
 - Very useful to understand system issues with sensor :
 - First assembled module has given similar performances than full ASIC testboard _
 - Jitter (ASIC+sensor) ~ 25 ps at 10 fC with calibration pulse
 - Vth (ASIC+sensor) can be set at ~4 fC
 - Testbeam results to come to confirm performances on testbench
 - Poster from Huang Xing presenting phase shifter measurements
- Design of ALTIROC3 is on-going with identified improvements, submission end 2022
 - Leveraging on bunch crossing synchronicity, using highly skewed digital logic to reduce couplings on analog
 - Analog performances relies on floorplan (power distribution, grounding, IR drops, deepNwell) to minimize coupling between analog and digital power domains.
 - Fully triplicated digital logic for SEE hardness





TOA TDC





TDC Power consumption : 0,5 mW @ 10% occupancy

Differential shunt capacitor voltage-controlled delay cells

- **START** pulse comes first and initializes the TDC operation. **STOP** pulse follows the **START** with a delay that represents the time interval to be digitalized.
- At each tap of the Delay Line, STOP signal catches up to the START signal by the difference of the propagation delays
 of cells in Slow and Fast branches: i.e. 140ps 120ps = 20ps (LSB).
- The number of cells necessary for STOP signal to surpass the START signal represents the result of TDC conversion
- Cycling configuration used in order to reduce the total number of Delay Cells.
- TDC range is equal to 128 * 20 ps = 2.56 ns